

2016

Variable Spurious Noise Mitigation Techniques in Hysteretic Buck Converters

Mina Nashed
Iowa State University

Follow this and additional works at: <https://lib.dr.iastate.edu/etd>

 Part of the [Electrical and Electronics Commons](#)

Recommended Citation

Nashed, Mina, "Variable Spurious Noise Mitigation Techniques in Hysteretic Buck Converters" (2016). *Graduate Theses and Dissertations*. 15982.
<https://lib.dr.iastate.edu/etd/15982>

This Dissertation is brought to you for free and open access by the Iowa State University Capstones, Theses and Dissertations at Iowa State University Digital Repository. It has been accepted for inclusion in Graduate Theses and Dissertations by an authorized administrator of Iowa State University Digital Repository. For more information, please contact digirep@iastate.edu.

Variable spurious noise mitigation techniques in hysteretic buck converters

by

Mina Nashed

A dissertation submitted to the graduate faculty
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Major: Electrical Engineering

Program of Study Committee:
Ayman Fayed, Co-Major Professor
Nathan Neihart, Co-Major Professor
Randall Geiger
Chris Chong-Nuen Chu
Jiming Song

Iowa State University

Ames, Iowa

2016

Copyright © Mina Nashed, 2016. All rights reserved.

TABLE OF CONTENTS

	Page
LIST OF FIGURES	v
LIST OF TABLES	x
ACKNOWLEDGMENTS	xi
ABSTRACT	xii
CHAPTER 1 INTRODUCTION	1
1.1 Power Conversion in Mixed-Signal Systems	1
1.2 Motivation and Contributions	3
1.3 Thesis Organization	5
CHAPTER 2 DC-DC POWER CONVERSION SCHEMES	6
2.1 Linear Power Converters	6
2.2 Switched-Capacitor Power Converters	8
2.3 Switched-Inductor Power Converters	10
2.3.1 Method of Operation	10
2.3.2 Power Losses	12
2.3.3 Noise Performance	14
2.3.4 Voltage-Mode PWM Control	17
CHAPTER 3 HYSTERETIC BUCK CONVERTERS	21
3.1 Voltage-Mode Hysteretic Buck Converters	21
3.2 Current-Mode Hysteretic Buck Converters	24
3.3 Fixed-Frequency Hysteretic Buck Converters	26

CHAPTER 4	SPREAD-SPECTRUM TECHNIQUES IN SWITCHED-MODE	
	POWER SUPPLIES	29
4.1	Sigma-Delta Modulators	30
4.2	Frequency Hopping/Stepping	32
4.3	Random Carrier Frequency	36
4.4	Spur-Free Constant Cycle Frequency Hopping	38
CHAPTER 5	PROPOSED SPUR-FREE CURRENT-MODE HYSTERETIC	
	BUCK CONVERTER	43
5.1	Top-Level Implementation	43
5.2	Spur-Free Operation.....	44
5.3	Eliminating Inductor Current Imbalance	45
5.4	Reducing Switching Frequency Variations	48
5.5	Loop Stability and Compensation.....	48
CHAPTER 6	PROPOSED CIRCUIT-LEVEL REALIZATION AND	
	MEASUREMENT RESULTS	51
6.1	Circuit-Level Realization.....	51
6.1.1	The Spur-Free CCFH Hysteretic Controller	51
6.1.2	All-Digital Soft-Startup	55
6.1.3	Dead-Time Generator and Gate-Drivers.....	58
6.2	Measurement Results	60

CHAPTER 7 FUTURE WORK AND CONCLUSION	80
7.1 Spur-Free Current-Mode Hysteretic Boost Converter	80
7.2 Conclusion	83
REFERENCES	84

LIST OF FIGURES

	Page
Figure 1.1 A typical power conversion scheme in battery-operated mixed-signal SoCs	1
Figure 2.1 Generic block diagram of a linear power regulator	7
Figure 2.2 Switched-capacitor power converters: (a) Voltage halver, (b) Voltage doubler, and (c) Voltage inverter	9
Figure 2.3 Buck regulator: (a) Block diagram, and (b) Associated waveforms	11
Figure 2.4 Buck regulator block diagram including parasitic components and non-idealities	13
Figure 2.5 Circuit models for output voltage spectrum: (a) Ideal LC filter, and (b) RLC filter including non-idealities [27]	15
Figure 2.6 Voltage-mode PWM buck regulator: (a) Block diagram, and (b) Associated waveforms	18
Figure 2.7 Type-III compensation circuit schematic	19
Figure 3.1 Voltage-mode hysteretic buck converter: (a) Block diagram, and (b) Associated waveforms	22
Figure 3.2 Current-mode hysteretic buck converter: (a) Block diagram, and (b) Associated waveforms	25
Figure 3.3 A block diagram showing a frequency regulation loop used to maintain a constant switching frequency in hysteretic converters. The Phase Frequency Detector (PFD) is used to detect frequency errors and the filter is used to ensure stability	27

Figure 4.1	Block diagram of a buck regulator using a sigma-delta modulator	31
Figure 4.2	Output voltage spectrum using frequency hopping versus a single frequency	33
Figure 4.3	Block diagram of a buck regulator using frequency stepping	34
Figure 4.4	Block diagram of a buck regulator using pseudo-random frequency hopping	34
Figure 4.5	Sawtooth signal and duty-cycle disturbance for the technique proposed in [34]	35
Figure 4.6	Random carrier frequency (RCF) control block diagram [35]	37
Figure 4.7	Spur-free constant cycle frequency hopping (CCFH) control [36]: (a) Block diagram, and (b) Associated waveforms	39
Figure 4.8	Normalized fundamental spur magnitude versus the ratio of frequencies for $n = 10$	42
Figure 5.1	Top-level block diagram of the proposed current-mode hysteretic buck converter incorporating spur-free CCFH control	44
Figure 5.2	Key waveforms for: (a) Single-sided hysteretic band modulation, and (b) Dual-sided hysteretic band modulation	47
Figure 5.3	Type-II compensation network: (a) Circuit realization, and (b) Loop gain and phase responses	50
Figure 6.1	The proposed spur-free CCFH hysteretic controller: (a) Simplified schematic showing the glitch-free latching circuit, and (b) Transistor-level details of the hysteretic band generator with feedforward adaptive control	52

Figure 6.2	High-speed, low-offset comparator realization	53
Figure 6.3	Error amplifier circuit-level realization	54
Figure 6.4	Pseudo Random Number (PRN) generator using a 20-stage Linear Feedback Shift Register (LFSR).....	54
Figure 6.5	Conventional analog realization of a soft-startup circuit and its timing diagrams	56
Figure 6.6	Proposed all-digital soft-startup circuit and its timing diagrams.....	57
Figure 6.7	(a) Standard dead-time generator and gate drivers, and (b) Adopted architecture from [47] modified by adding Schmitt triggers to prevent glitches and false triggering.....	59
Figure 6.8	Circuit-level realization of the Schmitt trigger.....	60
Figure 6.9	Die photo of the proposed spur-free CCFH current-mode hysteretic buck converter with the main building blocks highlighted	61
Figure 6.10	Test setup used to characterize the proposed converter.....	63
Figure 6.11	Evaluation Printed Circuit Board (PCB) with its main components highlighted	64
Figure 6.12	Output voltage spectrum with spur-free CCFH disabled (i.e. single switching frequency) and with the proposed spur-free CCFH switching enabled. Input voltage 4.2 V, output voltage 1.8 V, load current 200 mA	65
Figure 6.13	Output voltage spectrum with spur-free CCFH disabled (i.e. single switching frequency) and with the proposed spur-free CCFH switching enabled. Input voltage 6.3 V, output voltage 1.2 V, load current 500 mA	66

Figure 6.14	Output voltage spectrum with: (a) CCFH between two frequencies that do not meet the spur-elimination condition, and (b) Spur-free CCFH between two frequencies that meet the spur-elimination condition. Operating conditions are noted on each figure.....	67
Figure 6.15	Switching node spectrum with: (a) Spur-free CCFH switching disabled (i.e. single switching frequency), and (b) Spur-free CCFH switching enabled	69
Figure 6.16	Spur-free CCFH switching disabled (i.e. single switching frequency): (a) Output voltage ripple, and (b) Low-frequency spectrum up to 5 MHz.....	70
Figure 6.17	Spur-free CCFH switching with single-sided band modulation: (a) Output voltage ripple, and (b) Low-frequency spectrum up to 5 MHz.....	71
Figure 6.18	Spur-free CCFH switching with dual-sided band modulation: (a) Output voltage ripple, and (b) Low-frequency spectrum up to 5 MHz.....	72
Figure 6.19	Output transient response to a 500-mA load step with: (a) Spur-free CCFH switching disabled (i.e. single switching frequency), and (b) Spur-free CCFH switching enabled. Input voltage 4.2 V, output voltage 1.8 V	74
Figure 6.20	Switching frequency versus input voltage at different output voltages with and without adaptive hysteretic band	75
Figure 6.21	Startup operation of the converter with: (a) A conventional analog soft-startup circuit, and (b) The proposed all-digital soft-startup. Input voltage 4.2 V, output voltage 1.8 V, load current 500 mA	76
Figure 6.22	Power conversion efficiency versus load current at different output voltages with and without the proposed spur-free CCFH switching. Input voltage 3.6 V	77
Figure 6.23	Power conversion efficiency versus load current at different output voltages with and without the proposed spur-free CCFH switching. Input voltage 4.2 V	78

Figure 7.1	(a) Current-mode hysteretic boost converter architecture proposed in [50], (b) Emulated ramp signal waveform.....	81
Figure 7.2	Proposed spur-free current-mode hysteretic boost converter	82
Figure 7.3	Output spectrum with: (a) A single hysteretic band, (b) Spur-free switching with 8 hysteretic bands operating at 2.7V input, 3.6V output, 300mA load. (c) A single hysteretic band and, (d) Spur-free switching with 8 hysteretic bands operating at 1.8V input, 3V output, 200mA load ...	82

LIST OF TABLES

	page
Table 6.1 Performance summary and comparison	79

ACKNOWLEDGMENTS

I would like to thank my adviser, Dr. Ayman Fayed, for his guidance and support throughout the course of this research. I couldn't have asked for a better mentor both professionally and personally. I also would like to thank Dr. Nathan Neihart for his rigorous technical courses and for graciously agreeing to serve as a co-adviser for the last month before my graduation as Dr. Fayed transitioned to Ohio State. I would also like to thank my committee members Dr. Randall Geiger, Dr. Chris Chu and Dr. Jiming Song for their valuable time and contribution.

In addition, I would also like to thank my friends, colleagues, the department faculty and staff for making my time at Iowa State University a wonderful experience. Moreover, I would like to thank Kilby Labs and the Microcontroller Business Unit at Texas Instruments for logistical support and NSF (ECCS-1559972) for financial support.

Finally, I would like to thank my family for their patience and support.

ABSTRACT

This work proposes a current-mode hysteretic buck converter with a spur-free constant-cycle frequency-hopping controller that fully eliminates spurs from the switching noise spectrum irrespective of variations in the switching frequency and operating conditions. As a result, the need for frequency regulation loops to ensure non-varying switching frequency (i.e. fixed spurs location) in hysteretic controllers is eliminated. Moreover, compared to frequency regulation loops, the proposed converter offers the advantage of eliminating mixing and interference altogether due to its spur-free operation, and thus, it can be used to power, or to be integrated within noise-sensitive systems while benefiting from the superior dynamic performance of its hysteretic operation. The proposed converter uses dual-sided hysteretic band modulation to eliminate the inductor current imbalance that results from frequency hopping along with the output voltage transients and low-frequency noise floor peaking associated with it. Moreover, a feedforward adaptive hysteretic band controller is proposed to reduce variations in the switching frequency with the input voltage, and an all-digital soft-startup circuit is proposed to control the in-rush current without requiring any off-chip components. The converter is implemented in a 0.35- μm standard CMOS technology and it achieves 92% peak efficiency.

CHAPTER 1

INTRODUCTION

This chapter discusses a brief overview of the main aspects and challenges of power conversion schemes in mixed-signal systems and illustrates the main motivation and contribution of this work. The thesis organization is outlined at the end of the chapter.

1.1 Power Conversion in Mixed-Signal Systems

With the growing demand for integrating digital, analog, and radio frequency (RF) sub-systems together in a single system-on-chip (SoC), power delivery to these diverse functions within an SoC has become more complex than ever [1]. A typical battery-operated mixed-signal SoC is shown in Fig. 1.1 where power conversion circuits are now required to feature even faster dynamic operation, better power efficiency, smaller footprint, and reduced cost. Powering analog and RF sub-systems presents an additional challenge due to their stringent low noise requirements. Linear power regulators are more likely to achieve smaller footprint, reduced cost and is more suitable for powering noise-sensitive loads due to their low noise spectrum. However, buck converters continue to be preferred due to their much better power efficiency over a wide range of operating conditions at the expense of their spurious switching noise spectrum [2]. Since the power train and passive components in buck converters are determined mainly by the load demand, the differentiating factor between one design and another lies in the choice of the control topology that meets the demand for faster dynamic operation and reduced cost. The most common realization of a buck converter typically employs a pulse width modulation (PWM) control scheme for medium and heavy loading conditions. A type-III compensation network is typically used to ensure the converter's stability requiring a large number of off-chip passive components which adds to

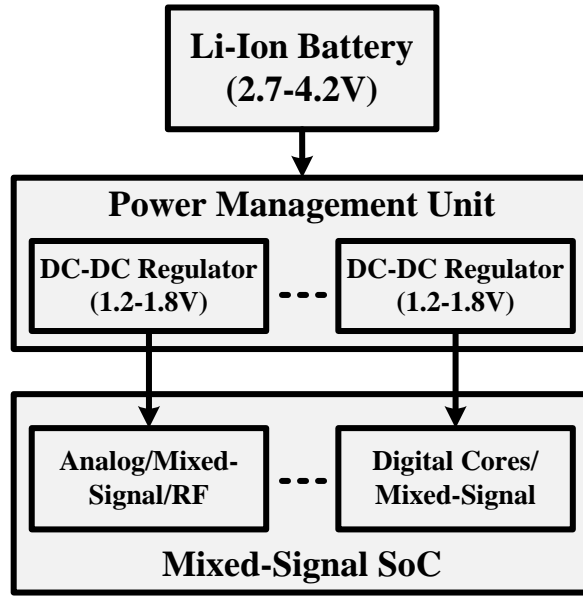


Figure 1.1 A typical power conversion scheme in battery-operated mixed-signal SoCs.

the overall cost and board area. Additionally, due to its average-based operation, transient performance is relatively slow in terms of recovery time due to the narrow bandwidth of the feedback loop [2].

While other alternative control architectures exist for implementing switching power converters, stringent transient response requirements to meet the fast changing load currents favor the choice of the hysteretic control topologies. Hysteretic controllers are attractive as they offer superior transient performance with a simple and cost-effective implementation due to their non-linear, inherently stable nature [3]. Nevertheless, hysteretic controllers have some drawbacks that must be carefully considered, most notably, they are self-oscillating with the switching frequency varying widely with operating conditions [3]. Thus, the tones (i.e. spurs) produced by the converter due to periodic switching will have highly variable locations. Spurs are a serious concern for noise-sensitive loads, such as RF and data converter circuits due to mixing and interference [4-6]. Moreover, integrating the converter

in SoCs, where the substrate, power/ground rails, and I/O rings are shared with many other circuits, compromises the system performance due to coupling of the spurs from the converter to these circuits. This problem is exacerbated when the location of the spurs is highly variable or cannot be precisely predicted.

1.2 Motivation and Contributions

Although hysteretic controllers enjoy many advantages in terms of cost-effective realization and superior dynamic performance, the variable spurs location prevents practical adoption of hysteretic topologies. Aiming at realizing a fixed spurs location (fixed switching noise spectrum) across different operating conditions, additional frequency regulation loops are traditionally employed. A frequency regulation loop senses the switching frequency then synchronizes the power converter to a reference clock by adjusting one of the design parameters of the controller (i.e. hysteretic band, bias current, etc...). Several flavors of frequency regulation loops have been proposed in the literature [7-15] and employed in some industrial implementations [16, 17] to mitigate the issue of switching frequency variability in hysteretic controllers using either digital or analog implementations and targeting both current-mode and voltage-mode hysteretic power converters. The performance of the different frequency regulation loops varies in terms of the achieved accuracy, power consumption and added area overhead. However, the stability of such loops is non-trivial, and frequency compensation is needed such that its operation does not interfere with the operation of the main power regulation loop in addition to the added design complexity, power consumption and silicon area [18]. Moreover, although frequency regulation loops may result in fixed spurs location, spurious noise is still problematic in systems sensitive to mixing and interference [4-6]. As a result, a practical realization of hysteretic converters with

a frequency regulation loop negates many of the inherent advantages of hysteretic controllers to start with. Choosing a conventional control scheme with some added feature to enhance its transient performance might be a more attractive solution for system designers to opt for [19]. Thus, alternative techniques are needed to enable practical adoption of hysteretic controllers without suffering the overhead and drawbacks of frequency regulation loops.

This thesis proposes incorporating a switching technique within current-mode hysteretic buck converters that fully eliminates the spurious components of the switching noise at all nodes within the converter, thereby producing spur-free noise spectrum irrespective of the actual switching frequency of the converter or any variability in its operating conditions [20]. As a result, the need for frequency regulation loops for ensuring non-varying spurious noise is eliminated, and the simple and cost-effective implementation of hysteretic control can be preserved. The digital-friendly realization of the spur-free switching technique constitutes minimal power and footprint overhead. Moreover, compared to frequency regulation loops, the proposed converter offers the advantage of eliminating mixing and interference altogether due to its spur-free operation, and thus, it can be used to power, or to be integrated within noise-sensitive systems while benefiting from the superior dynamic performance of its hysteretic operation. The proposed converter uses dual-sided hysteretic band modulation to eliminate the inductor current imbalance that results from frequency hopping along with the output voltage transients and low-frequency noise floor peaking associated with it. A feedforward adaptive hysteretic band controller is proposed to reduce variations in the switching frequency with the input voltage. Additionally, an all-digital soft-startup circuit is proposed to limit in-rush current with no off-chip components.

1.3 Thesis Organization

The rest of this thesis is organized as follows: chapter 2 gives an overview of the different methods to perform DC-DC power conversion, namely linear regulators, switched capacitor power converters and inductor-based switching regulators where their method of operation, advantages and drawbacks are discussed. Chapter 3 discusses hysteretic power conversion schemes including voltage-mode and current-mode buck converters and hysteretic power converters employing frequency regulation loops. Chapter 4 gives an overview of the different spread-spectrum techniques used with switching power converters where the method of operation, advantages and limitations of each are illustrated. Chapter 5 discusses the system-level aspects of the proposed spur-free current-mode hysteretic buck converter while chapter 6 details the circuit-level realization, physical layout and measurement results. Chapter 7 includes the potential future work and conclusion.

CHAPTER 2

DC-DC POWER CONVERSION SCHEMES

The different schemes to perform DC-DC power conversion namely, linear power converters, switched-capacitor power converters and switching-mode (buck) power converters are discussed in this chapter. Their method of operation, characteristics and performance are highlighted.

2.1 Linear Power Converters

One of the common methods to perform DC-DC conversion using a relatively simple architecture is to use linear regulators. The operation of a linear power regulator can be explained using the generic structure depicted in Fig. 2.1. A linear regulator mainly consists of a pass device (a PMOS transistor is used as an example), feedback network, controller and a reference circuit (not shown in the figure). The output voltage (V_{out}) is sensed using the feedback network typically via a resistive voltage divider and fed back to the controller. The high gain amplifier and its compensation network constitute the controller which tunes the ON resistance of the pass device to regulate the current flow from the input voltage (V_{in}) such that the feedback signal (V_{fb}) is approximately equal to the reference voltage (V_{ref}) [21]. The reference circuit is realized using either a Zener diode or a bandgap circuit that generates a stable voltage across process, voltage and temperature (PVT) variations with limited current driving capability. As described, the regulated output voltage can only be lower in magnitude than the input voltage (i.e. $V_{out} < V_{in}$) which means that linear regulators can only be used as step-down converters with no capability of performing inversion or step-up. The power conversion efficiency of linear regulators (η_{linear}) can be derived as:

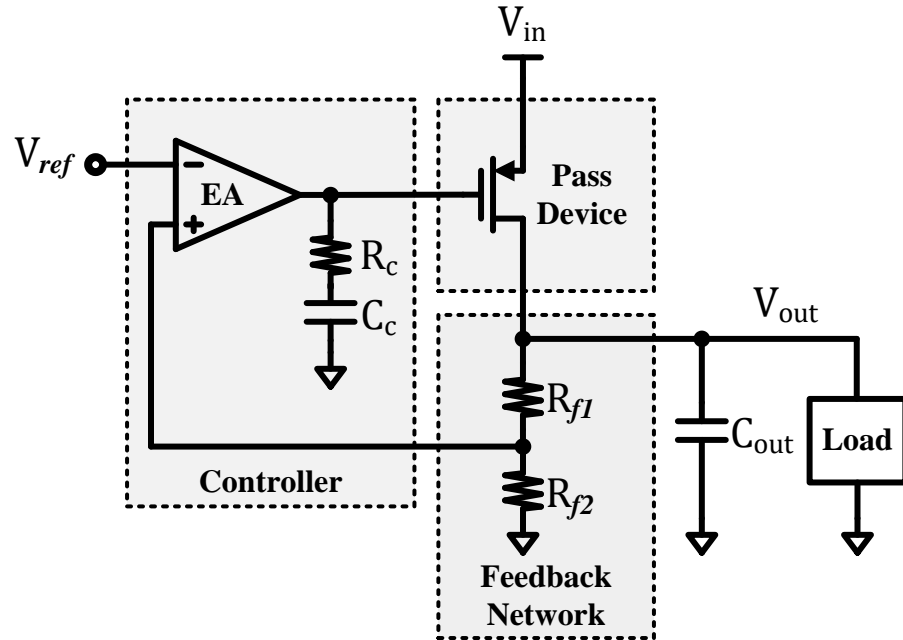


Figure 2.1 Generic block diagram of a linear power regulator.

$$\eta_{linear} = \frac{P_{out}}{P_{in}} = \frac{I_{out} \times V_{out}}{I_{in} \times V_{in}} \quad (2.1)$$

where P_{in}, P_{out} are the input and output powers while I_{in}, I_{out} are the input and output currents. Assuming I_{out} and I_{in} are equal, the maximum efficiency can be stated as:

$$\eta_{linear_max} = \frac{V_{out}}{V_{in}} \quad (2.2)$$

In a practical realization however, the controller circuitry consumes a finite amount of current which further degrades the efficiency. Thus, for a typical battery-operated system where both the input and output voltages vary significantly, choosing a linear regulator to perform power conversion can be very inefficient as efficiency depends primarily on the ratio of the output to input voltages. In specific applications where the difference in magnitude between V_{in} and V_{out} is small and remains almost constant, linear regulators can be useful and are then called low-dropout regulators (LDOs). The dropout voltage is defined as the

minimum voltage difference between V_{in} and V_{out} when the feedback loop fails to maintain power regulation [21].

Noise performance of linear regulators, however, is a huge advantage as they feature a significantly low noise profile (as compared to switching power converters) due to the fact that the method of operation in a linear regulator completely lacks any switching or periodic signal activity. The output noise of a linear regulator can be attributed to three main sources, namely, noise coupled through the substrate and supply rails, noise generated by the reference circuit and noise due to the physical layout of the converter. Choosing to use linear regulators can also be preferred for applications with very stringent noise requirements (sensitive analog and RF systems) while sacrificing power conversion efficiency [22].

2.2 Switched-Capacitor Power Converters

Another category of DC-DC converters is switched-mode power converters (SMPS) where the method of operation relies on periodic signal switching. The direct consequence of this periodic switching is spurious noise spectrum and larger time-domain ripple (as compared to linear regulators). Switched-capacitor power converters (SCPC) or charge-pumps are switching converters that consist of only switches and capacitors as energy storage elements. The lack of magnetic storage elements (inductors) enables integrating switched-capacitor converters fully on-chip although occupying significant silicon area [23]. SC converters can perform step-down, step-up and inversion of the input voltage. Fig. 2.2 depicts the topologies of a voltage halver, doubler and inverter where ϕ_1, ϕ_2 are non-overlapping clock phases controlling switches S_1 - S_4 and C_f, C_{out} are the flying and output capacitors respectively. The conversion ratio is determined by the circuit topology

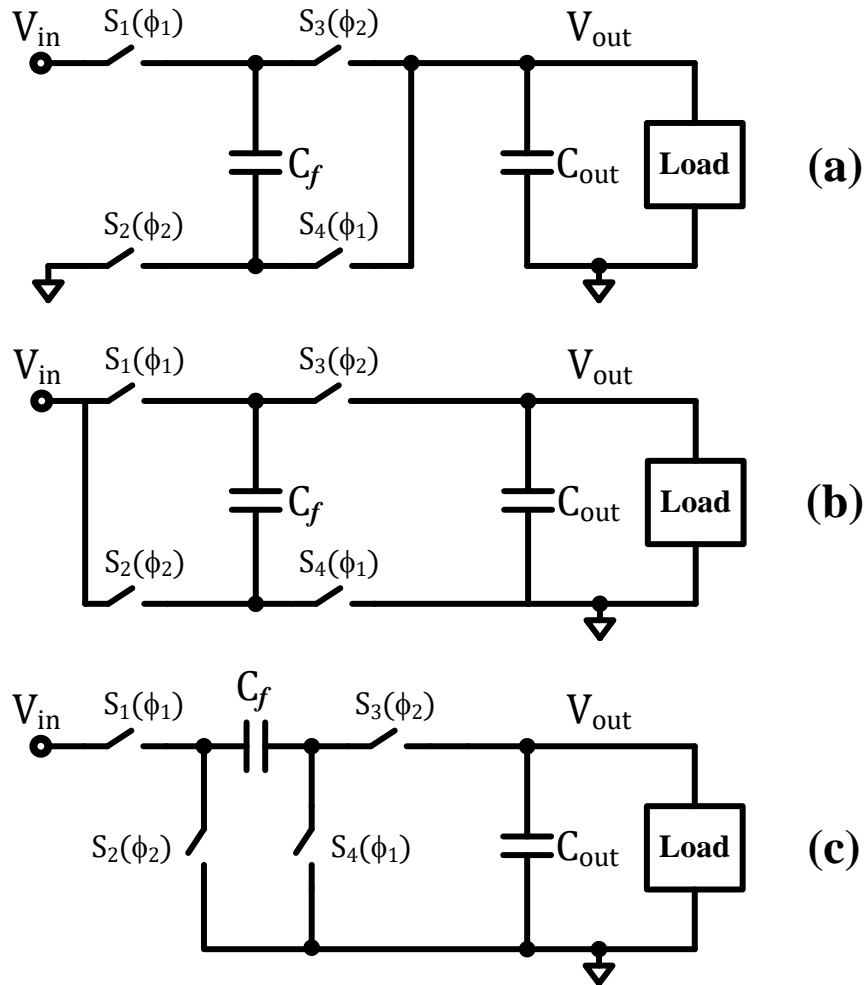


Figure 2.2 Switched-capacitor power converters: (a) Voltage halver, (b) Voltage doubler, and (c) Voltage inverter.

(i.e. the way capacitors and switches are connected and clocked) where the circuit should be re-arranged to achieve a different conversion ratio which limits the utilization of SC converters in applications with wide input and output voltage ranges. High power conversion efficiency can be achieved but only at specific voltage levels for a given topology. Typical applications include FLASH memories, LED lighting, LCD drivers and biomedical systems that require low current demand [24]. Different control schemes (hysteretic, frequency modulation, ... etc.) have been demonstrated to implement regulated (closed-loop) SC power converters [25-26].

2.3 Switched-Inductor Power Converters

Inductor-based converters are another type of switched-mode power converters and are the most widely used method for DC-DC power conversion. Switched-inductor power converters utilize both inductors and capacitors as energy storage elements and have the advantage of efficiently delivering wide range of load currents across wide input and output voltage ranges which is an attractive feature for battery-operated application. Step-down (buck), step-up (boost) and inverting topologies can be realized using inductor-based power converters [2]. The rest of this sub-section will focus on buck regulators where their fundamental method of operation, main sources of power loss, noise performance and pulse-width modulation control scheme are discussed.

2.3.1 Method of Operation

The basic structure of a synchronous buck regulator and its associated waveforms are shown in Fig. 2.3. The regulator consists of a high-side power switch (P-FET), a low-side power switch (N-FET), inductor (L), output capacitor (C), controller, non-overlap and driver circuits. The negative feedback loop aims at generating a square wave signal at the switching node (V_x) that has an average DC component equal to the reference voltage (V_{ref}) by adjusting either the ON-time (T_{on}) or the switching frequency (f_s) or both depending on the controller's architecture. The LC network then filters the AC components of the switching node generating a DC signal at the output (with a relatively small output voltage ripple) [2]. The inductor converts the square voltage wave into a triangular current wave with an up-slope of $(V_{in} - V_{out})/L$ and a down-slope of $(-V_{out}/L)$. The output capacitor then filters the inductor current's AC components, delivering the DC current to the load (I_L). When the inductor current is continuous during the whole switching period ($T_s = 1/f_s$), the regulator is

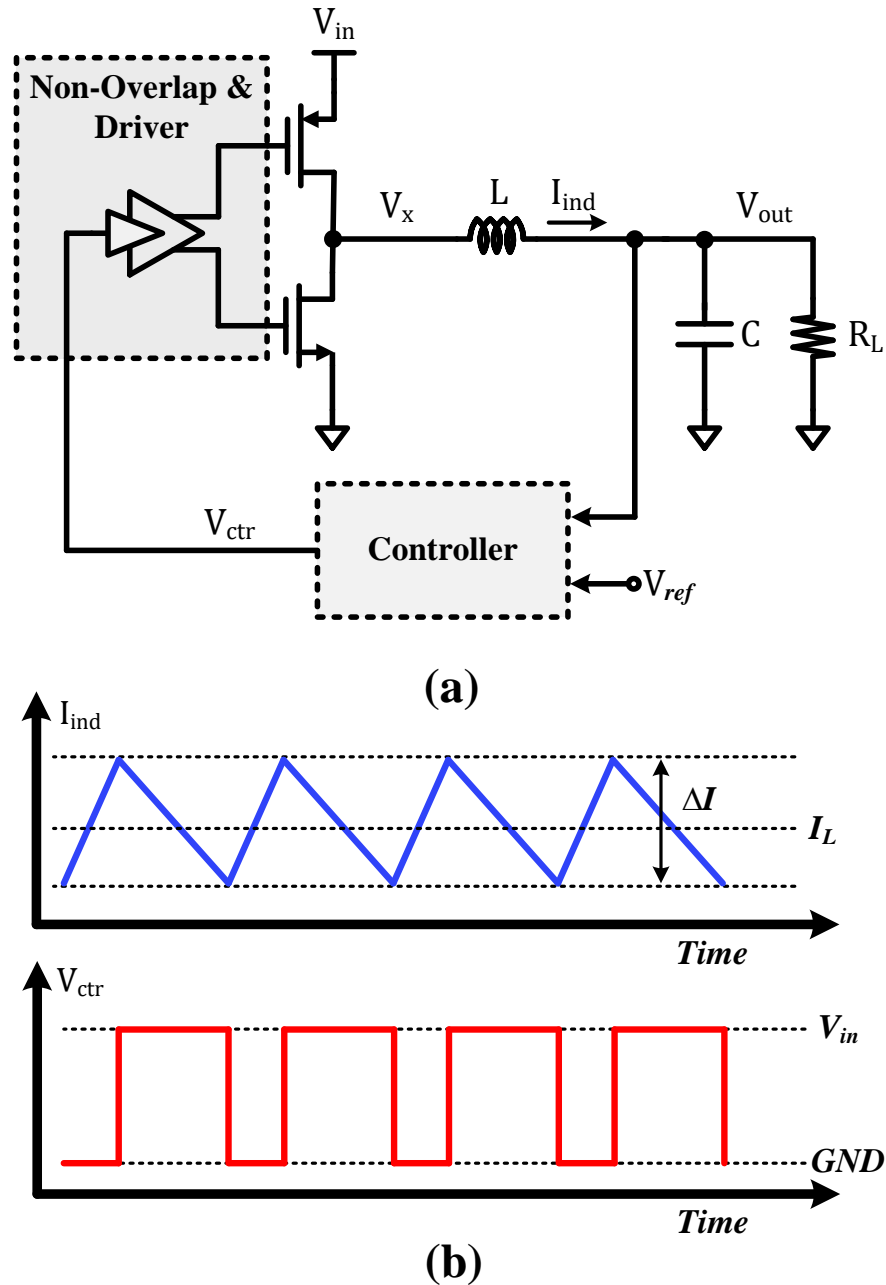


Figure 2.3 Buck regulator: (a) Block diagram, and (b) Associated waveforms.

said to be operating in the continuous conduction mode (CCM), whereas if it goes to zero for a certain interval of time, the regulator is said to be operating in the discontinuous conduction mode (DCM). As the work in this thesis doesn't target very low current demand, only operation in CCM will be considered in the rest of the dissertation.

The non-overlap and driver circuits provide a dead-time interval between the signals driving the high-side and low-side power FETs in order to avoid the shoot-through current. During the dead-time interval, the N-FET's parasitic body diode is forward-biased and the current continues to flow through the inductor in the same direction. The duty-cycle ($D = T_{on}/T_s$) can be related to the input voltage (V_{in}) and output voltage (V_{out}) during CCM operation as [2]:

$$D = \frac{V_{out}}{V_{in}} \quad (2.3)$$

The inductor current ripple (ΔI) and output voltage ripple (ΔV_{out}) can be stated as:

$$\Delta I = \frac{(V_{in} - V_{out})DT_s}{L} \quad (2.4)$$

$$\Delta V_{out} = \frac{\Delta I}{8f_s C} \quad (2.5)$$

Thus, for the same current and output voltage ripples, a higher switching frequency enables using smaller passives (L, C) saving cost and board area and for the same passives, a higher switching frequency results into smaller current and output voltage ripples.

2.3.2 Power Losses

The method of operation of an ideal buck regulator relies on energy transfer between magnetic and electric energy storage elements and thus, doesn't fundamentally incur any power losses. However, practical realization of the controller, driver circuits as well as components non-idealities cause power losses. Non-idealities include the power FETs' finite ON-resistance (R_{onP} for the P-FET and R_{onN} for the N-FET) and gate capacitances, inductor's parasitic DC resistance (R_{DCR}), output capacitor's parasitic equivalent series

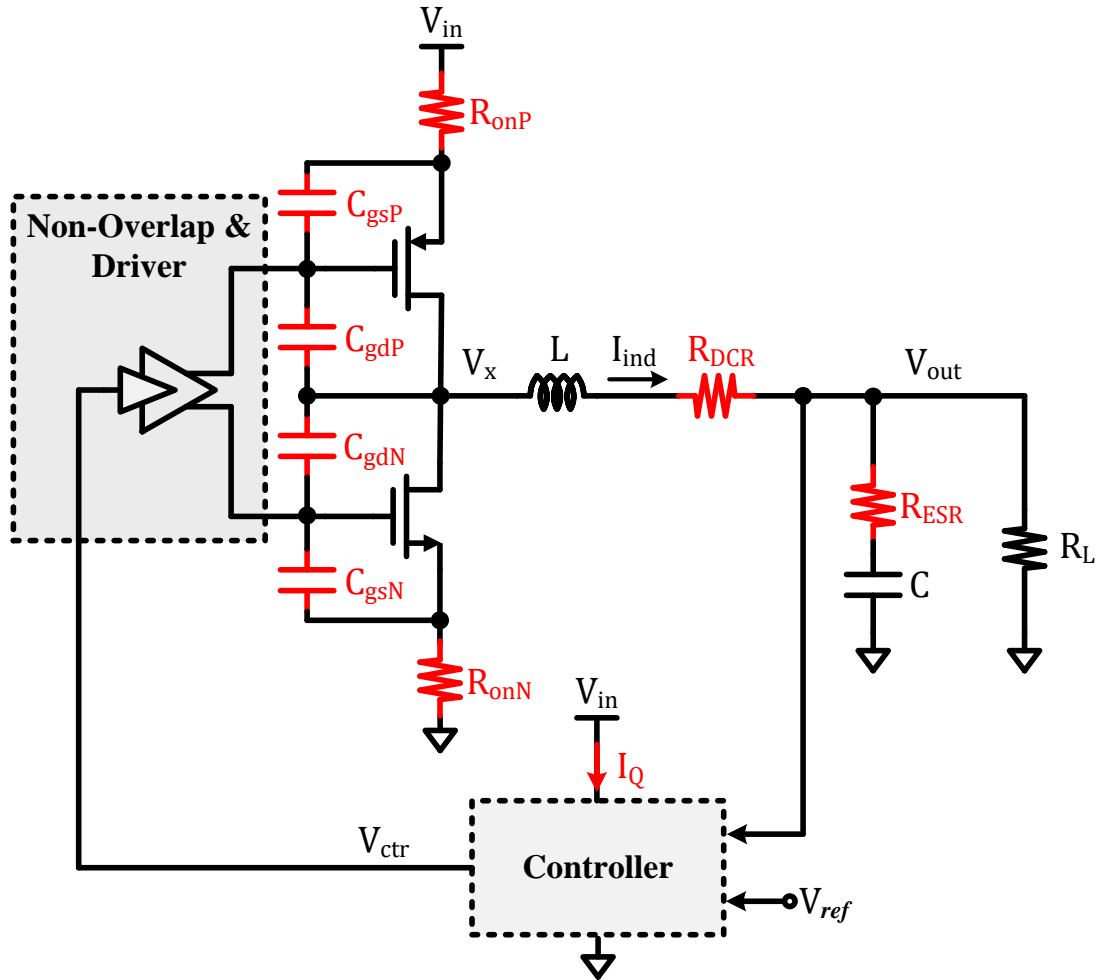


Figure 2.4 Buck regulator block diagram including parasitic components and non-idealities.

resistance (R_{ESR}) and the controller's quiescent current (I_Q) as shown in Fig. 2.4. The two main contributors to power loss in a buck regulator are conduction losses (P_{cond}) and switching losses (P_{sw}). Conduction losses are due to the finite resistance along the current's path where components that carry the full current waveform (both DC and AC portions) namely, the power FETs and inductor dissipate more conduction losses than components that only carry the AC portion (output capacitor). Assuming the power FETs are designed to have the same ON-resistance (i.e. $R_{onP} = R_{onN} = R_{on}$), conduction losses for a buck converter operating in CCM can be approximated as:

$$P_{cond} = (R_{on} + R_{DCR})I_L^2 + (R_{on} + R_{DCR} + R_{ESR})\left(\frac{\Delta I^2}{12}\right) \quad (2.6)$$

It is to be noted that due to the existence of the output capacitor's parasitic resistance, the output voltage ripple consists of both the ripple voltage across the capacitor (ΔV_C) and that across the resistor (ΔV_{ESR}) and can be stated as:

$$\Delta V_{out} = \frac{\Delta I}{8f_s C} + \Delta I R_{ESR} \quad (2.7)$$

Switching losses on the other hand refer to the power dissipated in the gate driver circuits to switch the power FETs that typically constitute a significant load capacitance due to their large sizes (to reduce their ON-resistance). The switching losses for a buck converter operating in CCM can be approximated as:

$$P_{sw} = V_{in}^2 (C_{gsP} + C_{gsN} + 2C_{gdP} + C_{gdN})f_s \quad (2.8)$$

where C_{gsP}, C_{gdP} are the gate-to-source and gate-to-drain capacitances of the P-FET while C_{gsN}, C_{gdN} are the gate-to-source and gate-to-drain capacitances of the N-FET. Thus, at higher loads, conduction losses become the dominant source of efficiency loss while at lighter loads, switching losses along with the controller's power loss become more dominant [2].

2.3.3 Noise Performance

Periodic switching in buck regulators results into spurious noise spectrum which is a limitation for usage in noise-sensitive applications. The switching node of the converter (V_X) is a periodic square wave that ideally swings between V_{in} and ground. Mathematical analysis to predict the spectral content of the output of a buck regulator operating in CCM regardless of the control scheme was conducted in [27]. The converter can be modeled as an open-

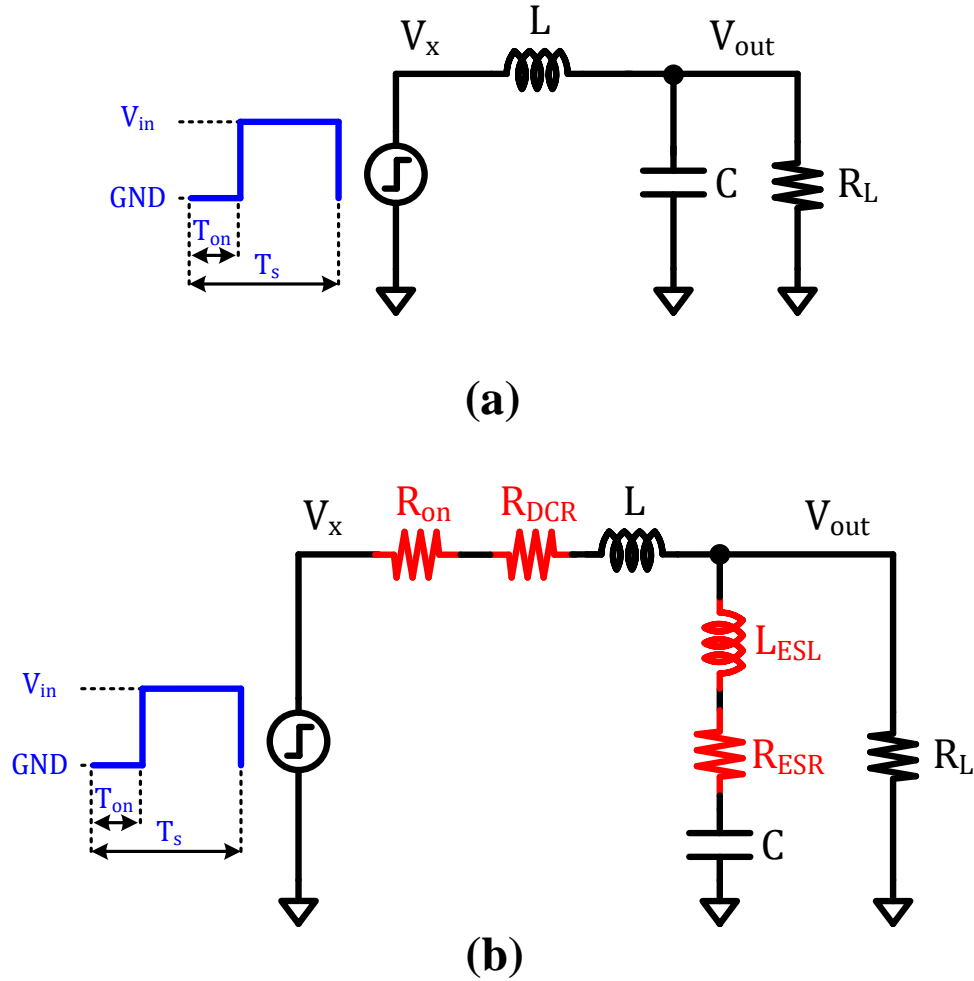


Figure 2.5 Circuit models for output voltage spectrum: (a) Ideal LC filter, and (b) RLC filter including non-idealities [27].

loop system where the switching node is square wave signal with a frequency of $f_s = \omega_s/2\pi$ and ON-time of T_{on} that feeds an LC network in the ideal case and an RLC network if non-idealities are included as shown in Fig. 2.5. As spurs exist only at the switching frequency and its harmonics, the output voltage spectral content of the k th harmonic can be stated as (assuming that the dead-time is significantly shorter than the switching period, which is typically the case in practical realizations) [27]:

$$|V_{out}(k\omega_s)| = |V_x(k\omega_s)| \times |H(k\omega_s)| \quad (2.9)$$

$$|V_x(k\omega_s)| = 4V_{in} \left| \frac{\sin\left(\frac{k\omega_s T_{on}}{2}\right)}{2\pi k} \right| \quad (2.10)$$

$$|H(k\omega_s)|_{LC} = \frac{1}{\left| (1 - (k\omega_s)^2 LC) + j(k\omega_s)\left(\frac{L}{R_L}\right) \right|} \quad (2.11)$$

$$|H(k\omega_s)|_{RLC} = \frac{\left(\frac{R_L}{R_L + R_T}\right) \times |(1 - (k\omega_s)^2 L_{ESL} C) + j(k\omega_s)(R_{ESR} C)|}{\left| \left(1 - \frac{(k\omega_s)^2 \alpha}{R_L + R_T}\right) + j(k\omega_s)\left(\frac{\beta - (k\omega_s)^2 L L_{ESL} C}{R_L + R_T}\right) \right|} \quad (2.12)$$

where $|V_x(k\omega_s)|$ is the spectral content of the switching node, $|H(k\omega_s)|_{LC}$ is the voltage divider transfer function for the ideal LC network, $|H(k\omega_s)|_{RLC}$ is the voltage divider transfer function for the non-ideal RLC network shown in Fig. 2.5, R_T is the sum of R_{on} and R_{DCR} , and L_{ESL} is the output capacitor's equivalent series inductance. The terms α and β are functions of the passive components and can be expressed as [27]:

$$\alpha = C(L_{ESL}R_L + LR_{ESR} + LR_L) \quad (2.13)$$

$$\beta = C(R_{ESR}R_L + R_T R_L + R_T R_{ESR}) + L \quad (2.14)$$

The model was verified using both simulation models and measurement results. Accounting for parasitic components and non-idealities revealed that higher order harmonics became more comparable to the fundamental and that all spurs are higher in magnitude than the ideal case. Moreover, it was shown that higher order harmonics don't decay as rapidly as in the ideal case mainly due to the parasitic components of the output capacitor that results into higher impedance and larger voltage ripple [27]. As a result, it can be concluded that spurious noise continues to be problematic even at frequencies much higher than the fundamental. Using post-linear regulation to filter the output ripple noise is traditionally

employed for noise-sensitive application at the expense of the degraded efficiency. However, with increasing the switching frequency of buck regulators in the MHz range rather than the traditional kHz range, typical linear regulators lose power supply rejection (PSR) at high frequencies and thus are ineffective in noise filtering [28].

Thus, alternative noise-reduction techniques have been proposed to facilitate integrating switching regulators in noise sensitive systems. Those techniques include time-domain methods that focus on reducing the output voltage ripple magnitude such as active ripple cancellation that works by injecting an AC signal with opposite polarity of the voltage ripple [29] or multi-phase control topologies that use a number of phases (inductors) to achieve a smaller current and voltage ripples at the expense of the added cost, area and design complexity overhead [30]. Other techniques rely on frequency-domain noise reduction techniques like sigma-delta modulators and spread-spectrum techniques [4-6, 31-38].

2.3.4 Voltage-Mode PWM Control

Pulse-width modulation (PWM) control is one of the most commonly used control architectures for buck regulators especially those operating in the continuous-conduction mode (medium to high load currents). The block diagram of a buck regulator utilizing a PWM controller is shown in Fig. 2.6 along with the associated waveforms. The controller consists of a feedback and compensation networks, sawtooth (or triangular) wave form generator, PWM comparator and non-overlap and driver circuits. The output voltage (V_{out}) is compared to the reference voltage (V_{ref}) using a high-gain error amplifier (to ensure good DC regulation) that generates an error signal (V_{err}), PMW comparator compares the sawtooth signal to the error signal and adjusts the pulse-width of the control signal accordingly (and thus the name, pulse-width modulation) [2].

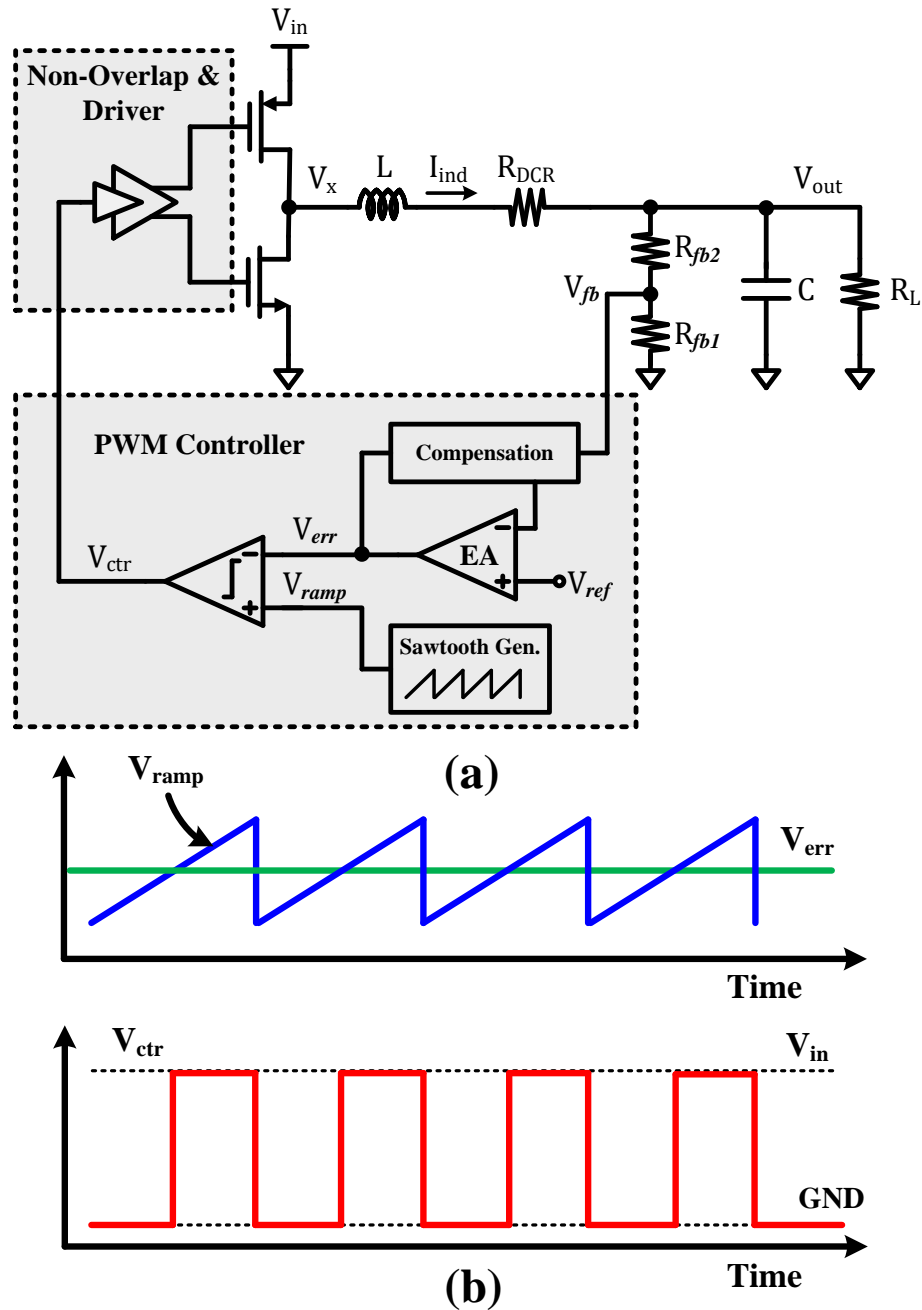


Figure 2.6 Voltage-mode PWM buck regulator: (a) Block diagram, and (b) Associated waveforms.

As the switching frequency of a PWM control architecture is constant (frequency of the sawtooth waveform generator), fixed switching noise spectrum is maintained (fixed spurs location) which is an advantage as compared to self-oscillating architectures where the switching frequency is variable across operating conditions [3].

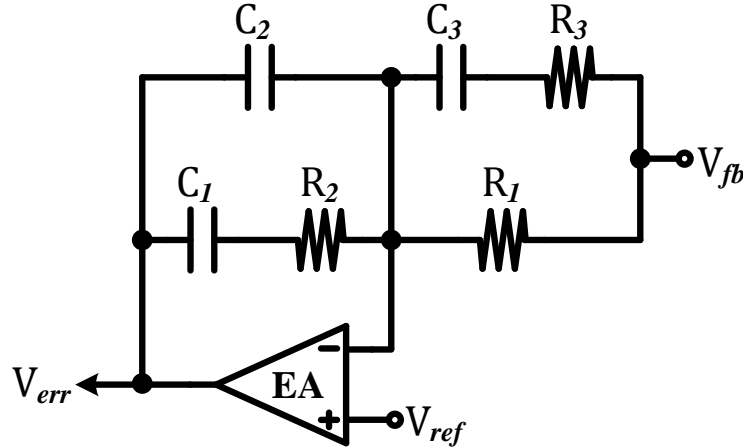


Figure 2.7 Type-III compensation circuit schematic.

Type-III compensation is traditionally used with PWM controllers to ensure loop stability. The circuit schematic of a type-III compensation network is shown in Fig. 2.7 and its transfer function can be stated as:

$$H(s) = \frac{V_{err}(s)}{V_{fb}(s)} = \frac{(1 + sR_2C_1)(1 + s(R_1 + R_3)C_3)}{sR_1(C_1 + C_2)(1 + sR_3C_3) \left(1 + sR_2 \left(\frac{C_1C_2}{C_1 + C_2}\right)\right)} \quad (2.15)$$

The transfer function of a type-III compensator features very high gain at low frequencies (good accuracy), two zeros to cancel the effects of the LC tank complex poles and two poles to suppress high frequency noise. Although type-III compensation achieves good stability in terms of phase margin, it requires a relatively large number of passives which are typically implemented as off-chip components leading to increased cost [2]. The closed-loop bandwidth of the regulator is typically designed to be around 10~20% of the switching frequency to make sure the loop will not react to the converter's ripple voltage and thus ensure stability. However, as an average-based control architecture, recovery time in reaction to a load step is inversely proportional to the closed-loop bandwidth. Thus, voltage-mode

PWM regulators typically feature a slow transient response for load and line steps. As a result, they are not typically preferred for applications requiring fast transient response which is becoming more important in mixed-signal SoCs.

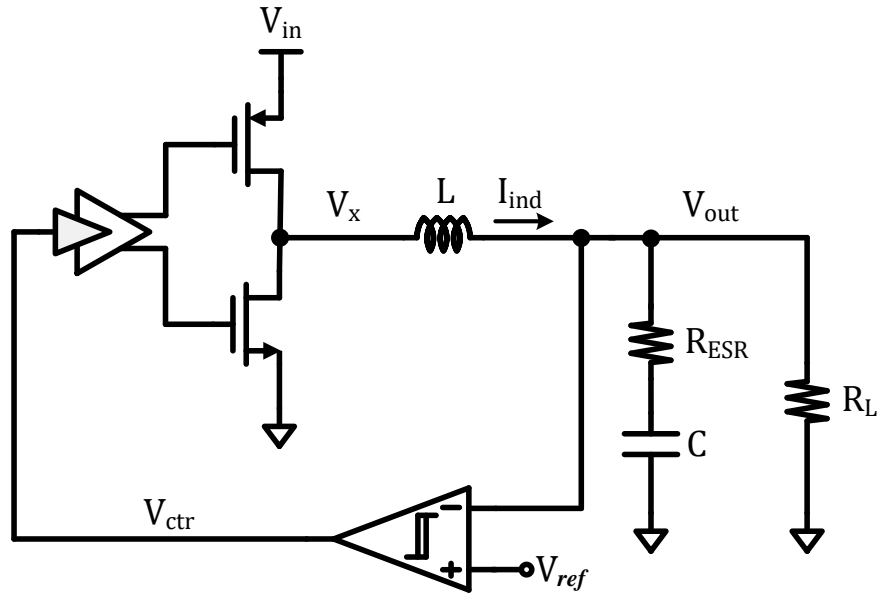
CHAPTER 3

HYSTERETIC BUCK CONVERTERS

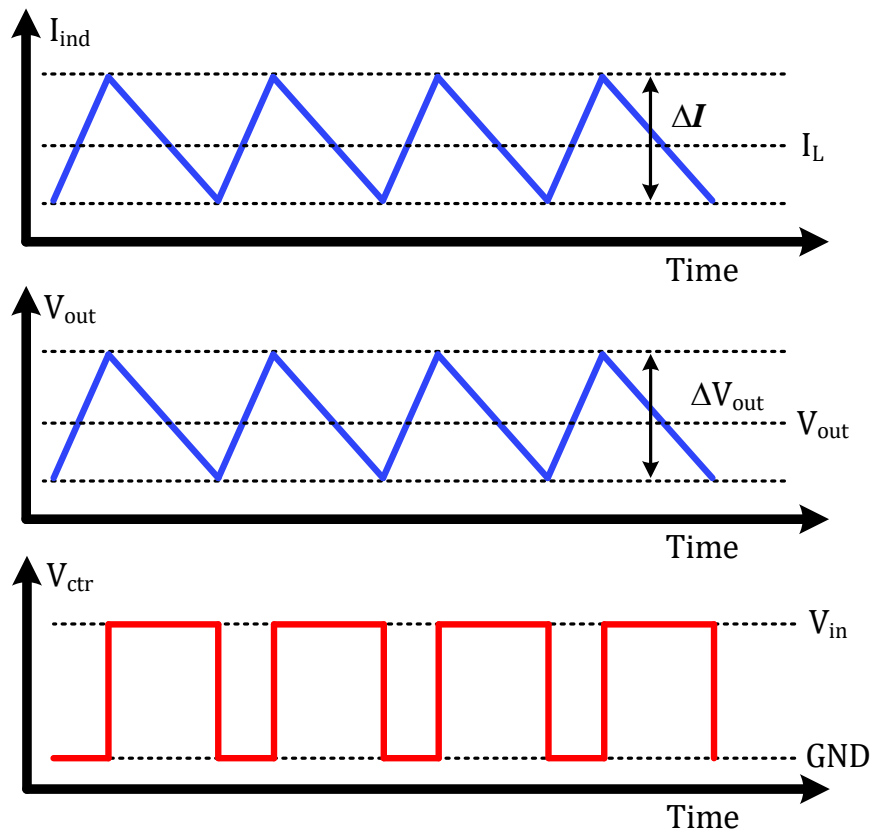
The characteristics, advantages and drawbacks of hysteretic control in buck converters are presented in this chapter. The method of operation of voltage-mode, current-mode hysteretic control as well as fixed-frequency hysteretic converters are illustrated in the following sub-sections.

3.1 Voltage-Mode Hysteretic Buck Converters

The block diagram of a voltage-mode hysteretic buck converter is shown in Fig. 3.1 along with the associated waveforms. The controller observes the output voltage ripple using a hysteretic comparator with a hysteresis band of V_{hys} that is being centered around the reference voltage (V_{ref}). As the output voltage magnitude raises above the upper threshold of the comparator ($V_{ref} + V_{hys}/2$), the controller turns OFF the P-MOS power FET allowing the voltage to drop until it reaches the lower threshold of the comparator ($V_{ref} - V_{hys}/2$) when the P-MOS power FET is turned back ON and the operation cycle repeats. An obvious observation about this control architecture is its simple structure which ideally consists only of a hysteretic comparator without the additional circuitry that is used in the conventional PWM controllers (i.e. error amplifier, compensation network and ramp generator) [3]. This advantage translates into smaller footprint, cost-effective realization and potentially low quiescent current consumption. Another advantage of the performance of hysteretic control schemes is the superior transient response which stems from the fact that the method of operation relies on the cycle-to-cycle changes in the value of the output voltage rather than its average which enables the converter to react much faster to load and line disturbances.



(a)



(b)

Figure 3.1 Voltage-mode hysteretic buck converter: (a) Block diagram, and (b) Associated waveforms.

Voltage-mode hysteretic control, however, suffers a number of serious limitations. The proper operation of the converter as described above assumes that the output voltage ripple is in phase with the inductor current ripple which is necessary for a stable operation. However, for this to be true, the output voltage ripple component due to the parasitic ESR resistance of the output capacitor should be the dominant source of ripple which implies that buck converters employing voltage-mode hysteretic control usually have larger output voltage ripple magnitude [3]. Furthermore, to fulfil the requirement on the minimum ESR value needed for a stable operation, an electrolytic capacitor is typically used. The speed specification of the hysteretic comparator is also critical to limit the delay (phase shift) introduced in the control loop which can affect the regulator's stability. Additionally, voltage-mode hysteretic converters are susceptible to noise coupling and other sources of distortion that might affect the shape of the output voltage ripple and thus cause false triggering of the hysteretic comparator.

Another major disadvantage of hysteretic controllers in general that limits their adoption in practical applications is having a switching frequency that varies across operating conditions. While the output voltage ripple is bounded within the hysteretic band (V_{hys}), its slope changes with the operating conditions. The switching frequency (f_s) of a voltage-mode hysteretic buck converter operating in CCM can be expressed as:

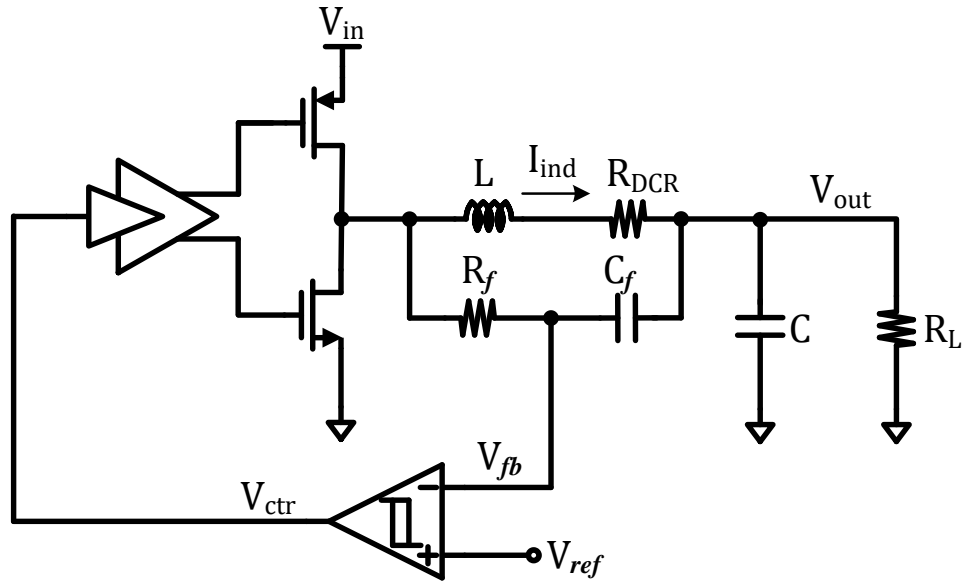
$$f_s = \frac{V_{in} R_{ESR} D(1 - D)}{L V_{in}} \quad (3.1)$$

where D is the duty-cycle. Thus, for applications with wide input and output voltage ranges which is typically the case in mixed-signal SoCs, the highly varying switching frequency can degrade the performance of noise-sensitive loads or even compromise the system integrity due to the noise coupled to other sub-systems through the shared power and ground rails.

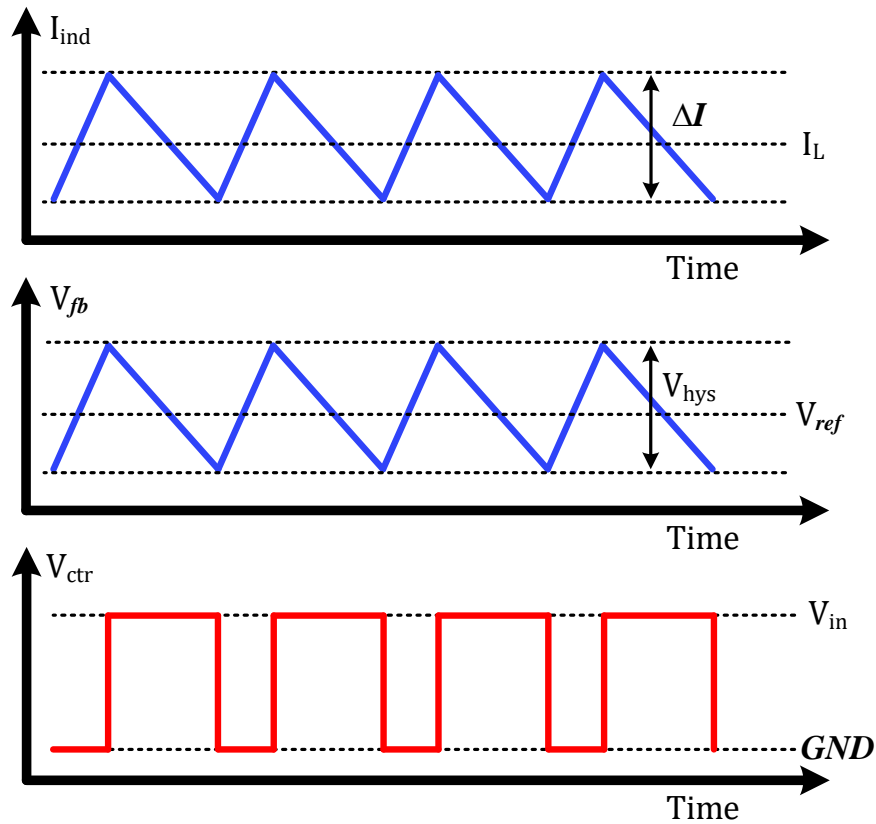
3.2 Current-Mode Hysteretic Buck Converters

The basic structure of a current-mode hysteretic buck converter is shown in Fig. 3.2 along with the associated waveforms. The control scheme utilizes the inductor current waveform as the ramp component for the feedback signal. The low-pass, current sensing RC filter integrates the voltage across the inductor to emulate the inductor current [3]. This method causes less loss and consumes less power than other passive and active current sensing techniques [39]. The feedback signal (V_{fb}) is a triangular voltage waveform that is in phase with the inductor current, and has a DC component equal to the output voltage (V_{out}) with an offset equal to the voltage drop across the parasitic DC Resistance (DCR) of the inductor. Although such offset degrades the DC load regulation of the converter, it can be mitigated by an additional high-gain voltage regulation loop as discussed in later chapters. The hysteretic comparator confines the feedback signal within the hysteretic band (V_{hys}) by turning OFF the P-MOS power FET once the feedback signal exceeds the upper bound of the hysteretic band ($V_{hys,H}$), and back ON once it drops below the lower bound ($V_{hys,L}$) as illustrated in Fig. 3.2(b). Unlike voltage-mode hysteretic topologies, current-mode hysteretic topologies are stable regardless of the ESR resistance of the output capacitor [15]. Therefore, ceramic capacitors with low ESR can be used to achieve small output voltage ripple. Moreover, since the swing of the feedback signal is not coupled to the output voltage ripple, the resolution and speed requirements of the hysteretic comparator can be significantly relaxed.

Current-mode hysteretic control enjoys the same advantages as in the case of a voltage-mode hysteretic control scheme in terms of its simple architecture, cost-effective realization and superior transient response. However, as a self-oscillating architecture,



(a)



(b)

Figure 3.2 Current-mode hysteretic buck converter: (a) Block diagram, and (b) Associated waveforms.

current-mode hysteretic control comes at the expense of a variable switching frequency. In fact, the switching frequency of the buck converter in Fig. 3.2(a) can be expressed as [9]:

$$f_s = \frac{D(1-D)}{\tau_{RC}(V_{hys}/V_{in}) + \tau_D} \quad (3.2)$$

where D is the duty-cycle of the control signal (V_{ctr}), V_{in} is the input voltage, V_{hys} is the comparator's hysteretic band, τ_{RC} is the time-constant of the current sensing filter and τ_D is the total loop delay (i.e. due to the comparator, the gate-drive circuit, and the power switches). Since the input and output voltages typically vary within a specified range, while the loop delay, the filter's time constant, and the comparator's hysteretic band vary with process and temperature, the switching frequency becomes dependent on the operating conditions. As a result, integrating current-mode controlled buck converters within noise sensitive systems can be challenging similarly as in the case of a voltage-mode hysteretic buck converter.

3.3 Fixed-Frequency Hysteretic Buck Converters

The variable switching noise profile of hysteretic converters can be a serious performance and reliability concern. The performance of noise sensitive loads like high precision analog and RF communication circuits can be degraded due to the variable switching noise [6]. Moreover, the spurious nature of the switching noise can compromise the operation of other sub-systems that share the same power and ground rails due to potential coupling and resonance with parasitic tank circuits. Switching frequency synchronization to an external reference clock is typically needed for a practical application of hysteretic control. An outer frequency regulation loop employing negative feedback as shown in Fig. 3.3 is used to set the switching frequency equal to the reference clock [11].

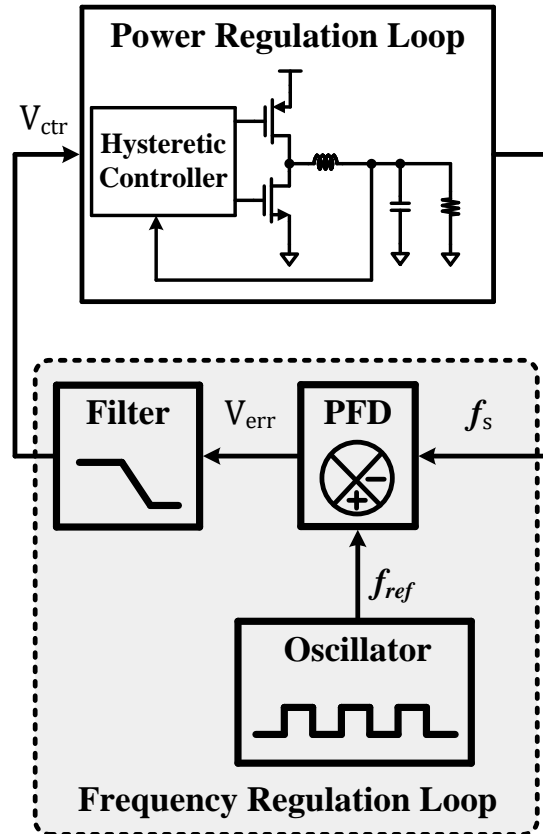


Figure 3.3 A block diagram showing a frequency regulation loop used to maintain a constant switching frequency in hysteretic converters. The Phase Frequency Detector (PFD) is used to detect frequency errors and the filter is used to ensure stability.

The method of operation is similar to that of a phase locked loop (PLL) where the converter's switching frequency is sensed and compared to the reference clock using a phase-frequency detector (PFD) producing an error signal. The output of the PFD is filtered, generating the control signal which adjusts a specific design parameter (hysteretic window, bias current or driver delay) in order to set the switching frequency to the desired value. Detailed small-signal modeling of the switching regulator similar to that of a voltage controlled oscillator (VCO) should be developed to analyze the stability of the frequency control loop such that its operation doesn't interfere with the main power regulation functionality of the converter [12, 18]. Furthermore, proper frequency compensation networks may be required to guarantee

loop stability. Several flavors of frequency control loops have been proposed in the literature using either digital or analog implementations and targeting both current-mode and voltage-mode hysteretic power converters [7-15]. The performance of the different frequency control loops varies in terms of the achieved accuracy, power consumption and added area overhead.

A careful investigation of the system-level diagram of the hysteretic power converter with the frequency control loop included reveals that many of the inherent advantages of hysteretic control had been negated. The design of a PLL is a huge overhead in terms of complexity, added power consumption and area overhead aside from implementing the power converter itself. In addition, stability is now an issue that should be rigorously investigated with potential added compensation needed. Implementing a conventional control scheme with some added feature to enhance its transient performance might be a more attractive solution for system designers to opt for. Furthermore, although a frequency control loop results in a predictable spectrum of the output voltage, the spurious switching noise can still degrade the performance of noise sensitive analog and RF loads if directly powered from the switching converter. As a result, a technique to mitigate the variable switching noise in hysteretic power converters without compromising neither the performance specifications nor the inherent advantages of hysteretic controllers is highly desirable.

CHAPTER 4

SPREAD-SPECTRUM TECHNIQUES IN SWITCHED-MODE POWER SUPPLIES

Noise reduction techniques employed in switched-mode power supplies to facilitate their integration in noise-sensitive systems can be divided into time-domain and frequency domain techniques. Time-domain techniques target reducing the actual magnitude of the inductor current and output voltage ripples using either multi-phase control architectures or active ripple cancellation techniques. Multi-phase control architectures utilize multiple inductors per regulator with their phases accurately spaced in time such as to reduce (or cancel at specific duty-cycles) the current ripple [30]. Precise control is critical to ensure effective current ripple cancellation which is an implementation overhead. A more significant overhead is the added components' cost and board area due to the extra inductors used [30]. Active ripple cancellation techniques utilize a linear regulator to supply an AC cancelling signal that is out of phase with the inductor current ripple [29]. Although the linear regulator doesn't supply a DC current; however, a wide bandwidth topology is needed for good ripple cancellation which degrades the overall power conversion efficiency. Moreover, phase delay between the cancelling signal and the inductor current ripple should be tightly controlled.

Frequency-domain noise reduction techniques on the other hand rely on spreading the spurious energy in the frequency-domain across a dithering band or a number of discrete frequencies rather than a single tone. These techniques generally provide better tradeoff between spurious noise reduction and implementation complexity and overhead. The challenge, however, is the design of the spreading method in order to maximize noise reduction while maintaining other performance aspects of the power converter such as

efficiency, transient response and output voltage ripple. An overview of different spread-spectrum techniques is going to be discussed in the rest of this chapter.

4.1 Sigma-Delta Modulators

Sigma-delta ($\Sigma\Delta$) modulators have been traditionally used in over-sampling analog-to-digital data converters (ADCs) as a method of improving the signal-to-noise ratio (SNR). In switched-mode power supplies, $\Sigma\Delta$ modulators have been used as a control scheme for low-noise applications. Incorporating a $\Sigma\Delta$ modulator in a buck regulator is rather straightforward from a block-level perspective as it replaces the PWM modulator as shown in Fig. 4.1 [31, 32]. The $\Sigma\Delta$ modulator works by injecting random quantization noise in the control loop to reduce spurs, then use noise shaping to push the quantization noise to higher frequencies. Ideally, the LC tank would filter those high frequency noise contents; however, due to parasitic components and non-idealities, LC filter attenuation at higher frequencies is much less than the ideal case (as discussed in chapter 2). As a result, $\Sigma\Delta$ modulators practically result in excessively high random noise floor due to the additional quantization noise [31]. Moreover, noise feedthrough and coupling in practical realizations due to the modulator's sampling clock also adds to the noise floor at higher frequencies. The sampling frequency (f_{sample}) can be expressed in terms of the switching frequency (f_s) as [32]:

$$f_{sample} = d \times f_s \quad (4.1)$$

where d is a scaling factor that can be expressed in terms of the duty-cycle ($D = V_{out}/V_{in}$) as:

$$d = \begin{cases} 1/D, & D \leq 0.5 \\ (1 - D)/D, & D > 0.5 \end{cases} \quad (4.2)$$

In the time-domain, $\Sigma\Delta$ modulators generate a pulse-code-modulation (PCM) control waveform that consists of a sequence of logic high and logic low pulses with an average

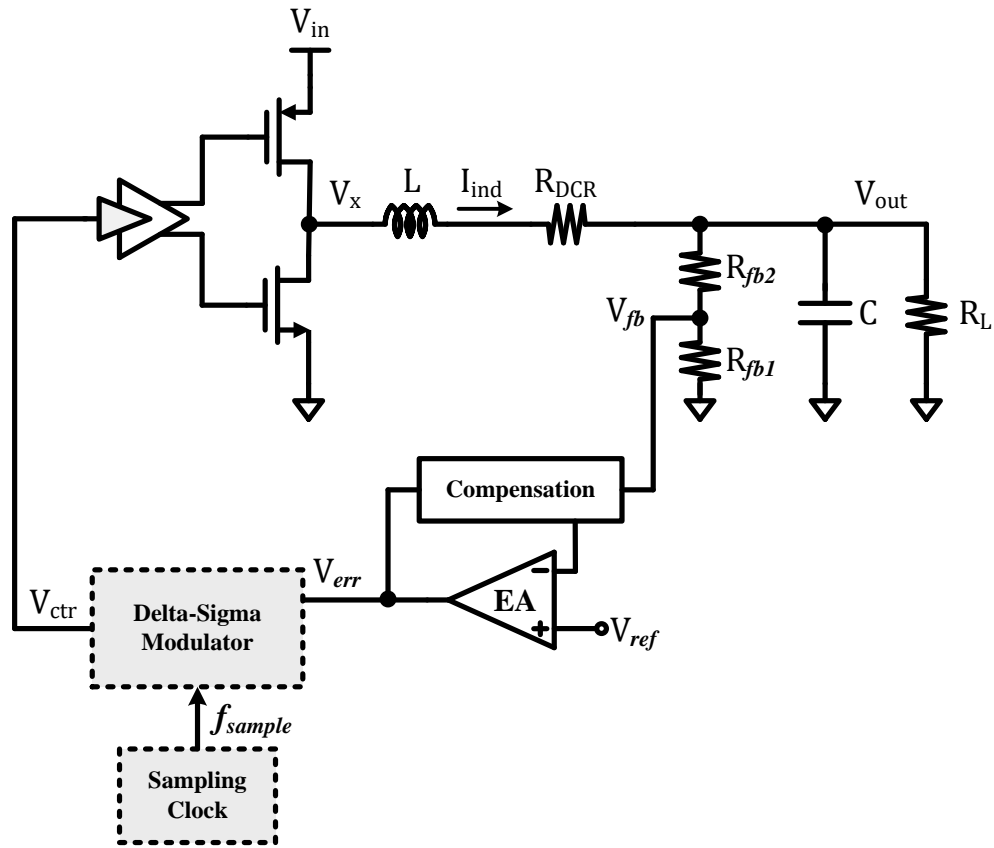


Figure 4.1 Block diagram of a buck regulator using a sigma-delta modulator.

equal to the reference voltage. This control waveform doesn't have a deterministic duty-cycle and thus, duty-cycle disturbances lead to larger output voltage ripple and transients [31]. Utilizing multi-bit $\Sigma\Delta$ modulators have been proposed to further improve the noise performance; however, such realizations suffer added cost and board area due to the extra inductors needed [32].

The operation of $\Sigma\Delta$ modulators as a control scheme for switched-mode power supplies inherently rely on an average-base architecture. Therefore, they are not suitable to be used in self-oscillating control architectures such as hysteretic controllers where the switching frequency varies across operating conditions and rely in its operation on the cycle-to-cycle value of the controlled signal rather than its average.

4.2 Frequency Hopping/Stepping

Frequency hopping/stepping is a different category of frequency-domain techniques for noise reduction in switched-mode power supplies where the switching frequency is changed over time. Assuming a discrete number of frequencies ($f_{s(1)}, f_{s(2)}, \dots, f_{s(N)}$), the spurious energy of the fundamental tone is spread across the N frequencies (N smaller spurs) where the fundamental spur reduction is ideally $20 \log N$ as shown in Fig. 4.2. Reported measured reduction, however, is a function of the hopping rate and the selection of the frequencies [4, 5]. The fundamental method of operation of frequency hopping/stepping techniques doesn't inherently add any extra noise to the power regulator (unlike $\Sigma\Delta$ modulators). Instead, the spurious energy is spread in-band around the different frequencies without causing high frequency noise floor peaking. Also, a general feature of frequency hopping/stepping techniques is that they don't require a lot of overhead in terms of design complexity, area or power as compared to time-domain noise reduction techniques or $\Sigma\Delta$ modulators. The power conversion efficiency of the converter can be maintained if switching power losses calculations were based on the average switching frequency as well as minimizing the extra quiescent current used to implement the frequency dithering algorithm. Duty-cycle disturbances, however, are generally a drawback in power regulators utilizing frequency hopping/stepping techniques. The amount of duty-cycle disturbances and the associated output voltage transients is a function of the controller's architecture and frequency hopping algorithm implemented [4, 5].

A realization example that avoids large duty-cycle disturbances is shown in Fig. 4.3 where a digital-to-analog (DAC) converter is used to increment/decrement the switching frequency generating a triangular waveform of the switching frequency versus time with a

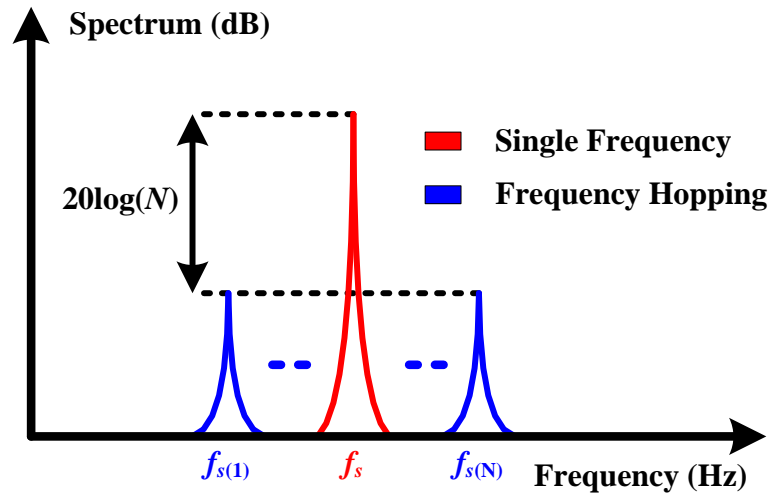


Figure 4.2 Output voltage spectrum using frequency hopping versus a single frequency.

modulation frequency of f_{mod} [33]. The small frequency steps limit the duty-cycle disturbances and output voltage transients when changing the switching frequency. However, as the frequencies are closely spaced, the effective spur reduction is reduced even when using a large number of frequencies as the residual energies of the smaller spurs overlap and add constructively. Moreover, as the frequency's triangular waveform is periodic, additional spurs are added to the noise spectrum at the modulation frequency (f_{mod}) which can cause an elevation in the low frequency noise content (modulation frequency is typically much lower than the switching frequencies) [33].

Another realization that aims at maximizing spur-reduction at the cost of duty-cycle disturbances is to use a pseudo-random number generator to randomly select the switching frequency from a bank of discrete frequencies as shown in Fig. 4.4. As the frequency waveform versus time is random (a pseudo-random number generator is actually periodic but with a time period that is very long as compared to practical spectrum observation windows), no extra spurs are added to the noise spectrum. However, a slow hopping rate is

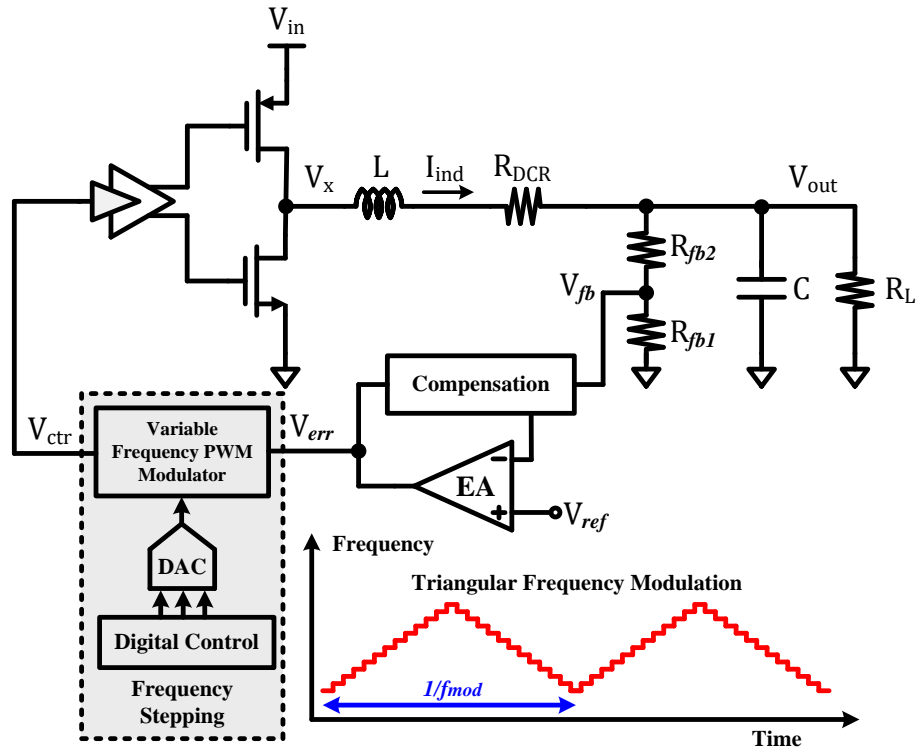


Figure 4.3 Block diagram of a buck regulator using frequency stepping.

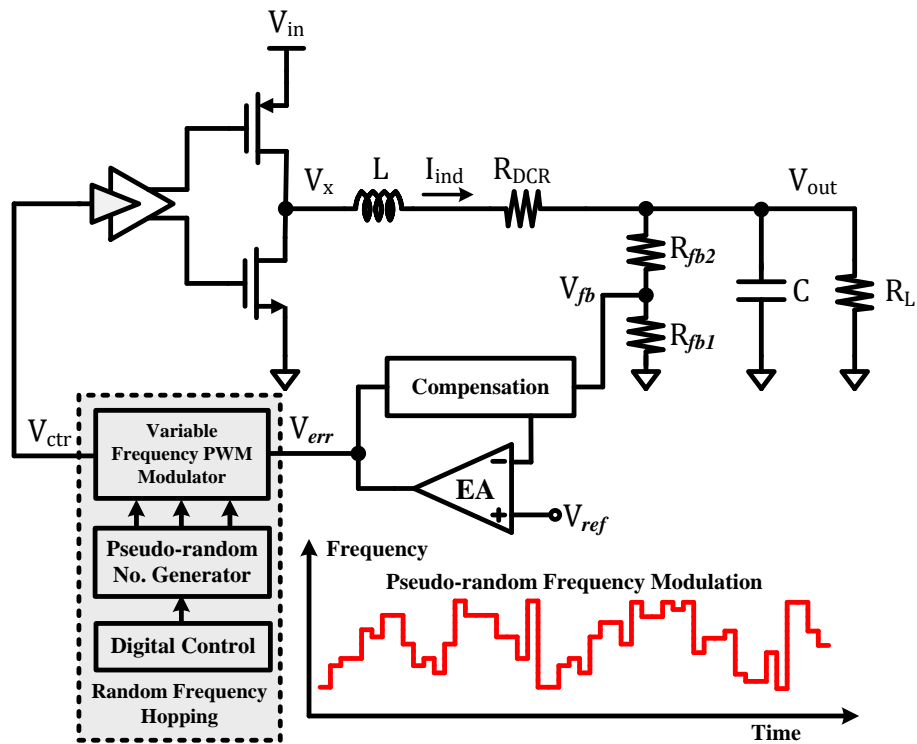


Figure 4.4 Block diagram of a buck regulator using pseudo-random frequency hopping.

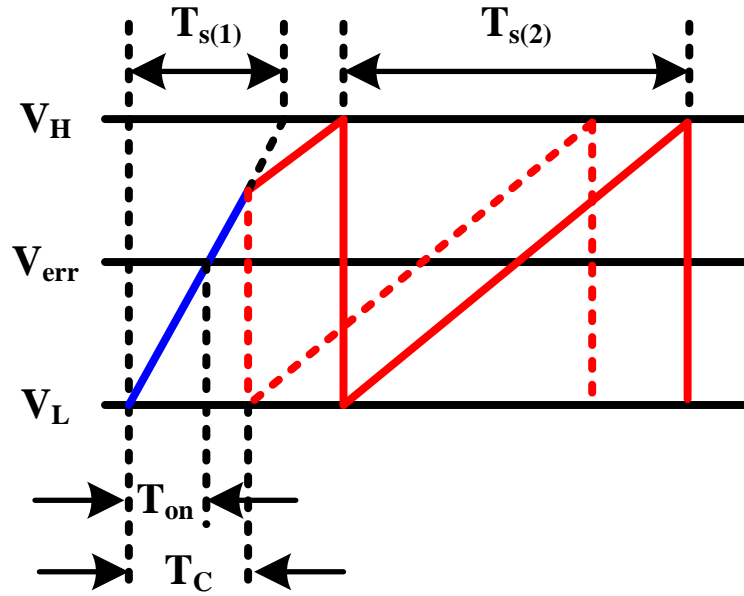


Figure 4.5 Sawtooth signal and duty-cycle disturbance for the technique proposed in [34].

usually practically used in order to fulfill the output voltage ripple requirements which degrades noise reduction. An improved asynchronous frequency hopping technique was demonstrated that lowered duty-cycle disturbances while enabling using fast hopping rates [34]. This technique relies on a PWM sawtooth ramp signal that swings between constant upper and lower thresholds (V_H and V_L) while the frequency is hopped by changing the voltage slope (changing the charging current through a fixed capacitor). Assuming the switching frequency changes from $f_{s(1)}$ to $f_{s(2)}$ (switching period of $T_{s(1)}$ to $T_{s(2)}$) after time T_C and that the sawtooth ramp signal is reset at that instance (goes to zero) as shown in Fig. 4.5, the duty-cycle can be expressed in terms of the ON time (T_{on}) and T_C as [34]:

$$D = \begin{cases} T_{on}/T_C, & T_{on} \leq T_C < T_{s(1)} \\ 1, & 0 < T_C < T_{on} \end{cases} \quad (4.3)$$

A simple modification of allowing the sawtooth ramp signal to continue with the new slope instead of being reset yields the following duty-cycle [34]:

$$D = \frac{T_{on}}{T_C + T_{s(2)}(1 - T_C/T_{s(1)})}, \quad 0 < T_C < T_{s(1)} \quad (4.4)$$

which shows much smaller variation as compared to the original case which enables a faster hopping rate while maintaining the output voltage ripple requirements.

4.3 Random Carrier Frequency

In an attempt to reduce duty-cycle disturbances while further reducing spurious noise, random carrier frequency (RCF) control was proposed [35]. The controller uses a voltage-controlled sawtooth signal generator that dithers the switching frequency as shown in Fig. 4.6. The switching frequency is only changed at the end of a full switching cycle which results into preserving the duty-cycle of the regulator independent of the frequency applied. In a practical realization, however, the duty-cycle will be adjusted by the controller to compensate for the varying switching losses among different switching frequencies which is still a minor effect. The control voltage is a true random white noise source implemented using a bipolar junction transistor (BJT) configured as a noise diode that gives constant signal strength over wide frequency band followed by a three stage amplifier [35]. At the end of a switching cycle, a sampling control triggers a sample-and-hold circuit to sense the noise source and as a result, change the switching frequency as shown in Fig. 4.6. Owing to its analog realization, the noise source dithers the switching frequency across a continuous range rather than discrete values which is effectively an infinite number of frequencies. Moreover, as duty-cycle disturbances are minimized, wide frequency range and fast hopping rate can be used without causing significant output voltage glitches while achieving a spur-free spectrum.

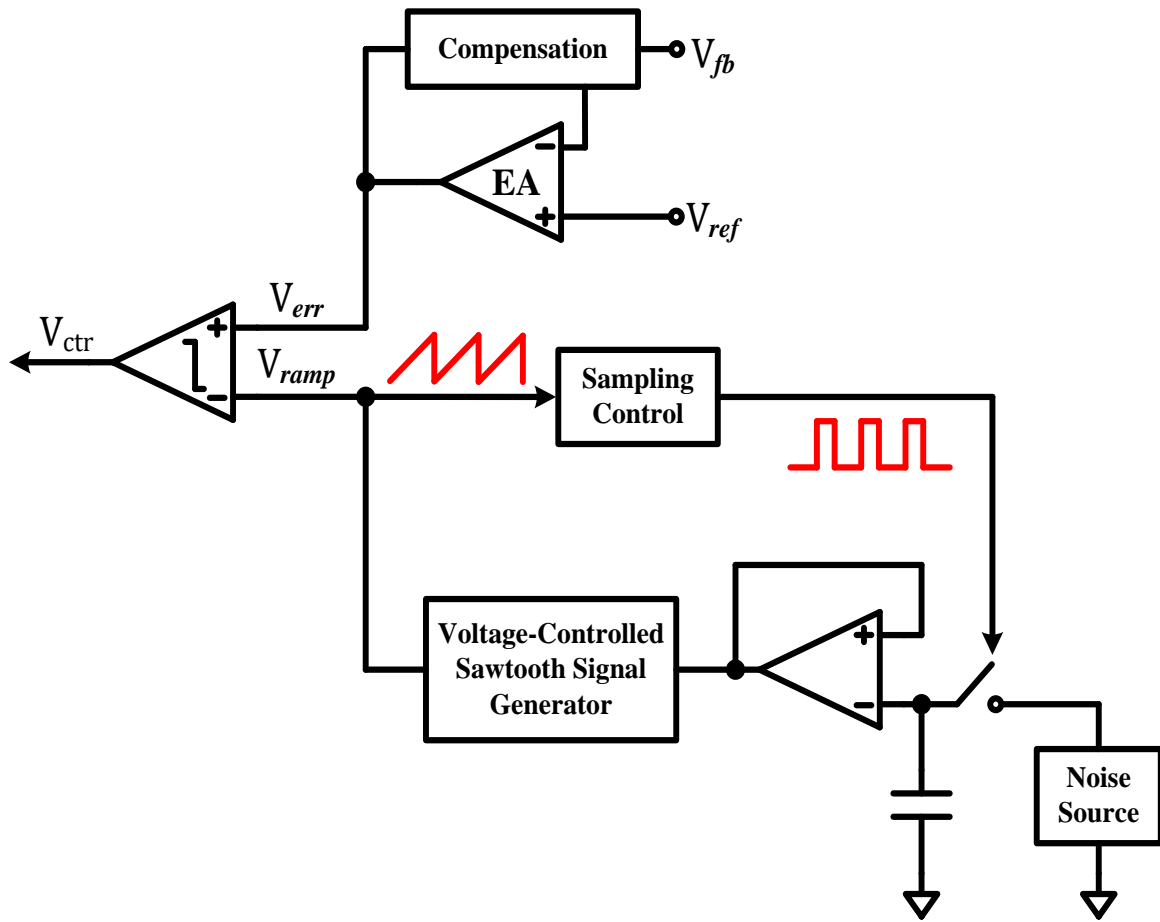


Figure 4.6 Random carrier frequency (RCF) control block diagram [35].

Although the random carrier frequency control generates a spur-free output spectrum as the spurious tones are spread across infinite number of switching frequencies and at the same time preserve the duty-cycle, the controller suffers a significant practical drawback. In fact, the controller realization represents a significant added design complexity and overhead in terms of area and power in addition to being prone to process, temperature and voltage (PVT) variations due to its analog nature which can lead to inconsistent performance. As a result, other techniques that can be realized in a digital friendly manner without significant overhead are highly desirable as noise reduction techniques in switched-mode power supplies.

4.4 Spur-Free Constant Cycle Frequency Hopping

A digital-friendly spur-free control technique utilizing a pseudo-random number generator was demonstrated with a PWM voltage-mode buck converter [36-37]. Spreading the switching frequency across a finite number of frequencies was shown to fully eliminate spurious tones given that relative ratios of frequencies used fulfill a spur-elimination condition. The type-III compensated PWM voltage mode buck converter employing constant cycle frequency hopping (CCFH) spur-free control and the associated waveforms are depicted in Fig. 4.7. The control signal V_{ctr} is used to trigger a digital pseudo-random number generator which in turn randomly selects the switching frequency from a finite set of values (only two frequencies $f_{s(1)}$ and $f_{s(2)}$ are used here for simplicity). Using V_{ctr} as the hopping signal instead of an external clock source in conjunction with fixing the PWM ramp signal swing results in minimizing duty-cycle disturbance [36]. A constant duty-cycle irrespective of the selected switching frequency suppresses time-domain voltage transients and glitches. More importantly, triggering the pseudo-random number generator every constant number of switching cycles results in a variable and random hopping period. This random hopping frequency effectively introduces the phase chopping necessary for full spur-elimination. As a new ramp cycle is started from scratch whenever the corresponding frequency is chosen, the pulse train experiences a phase shift relative to when the same frequency was last selected. This phase shift itself is also random due to the random selection of frequencies. Mathematically, the spurious component at the j th harmonic of the first switching frequency $f_{s(1)}$ can be stated as [36]:

$$\left(\frac{f_{s(2)}}{f_{s(1)} + f_{s(2)}} \right) \cdot \gamma_j \cdot \left[\begin{array}{l} \cos(2\pi j \cdot k \cdot f_{s(1)} \Delta T) \cdot \cos(2\pi j f_{s(1)} t) \\ + \sin(2\pi j \cdot k \cdot f_{s(1)} \Delta T) \cdot \sin(2\pi j f_{s(1)} t) \end{array} \right] \quad (4.5)$$

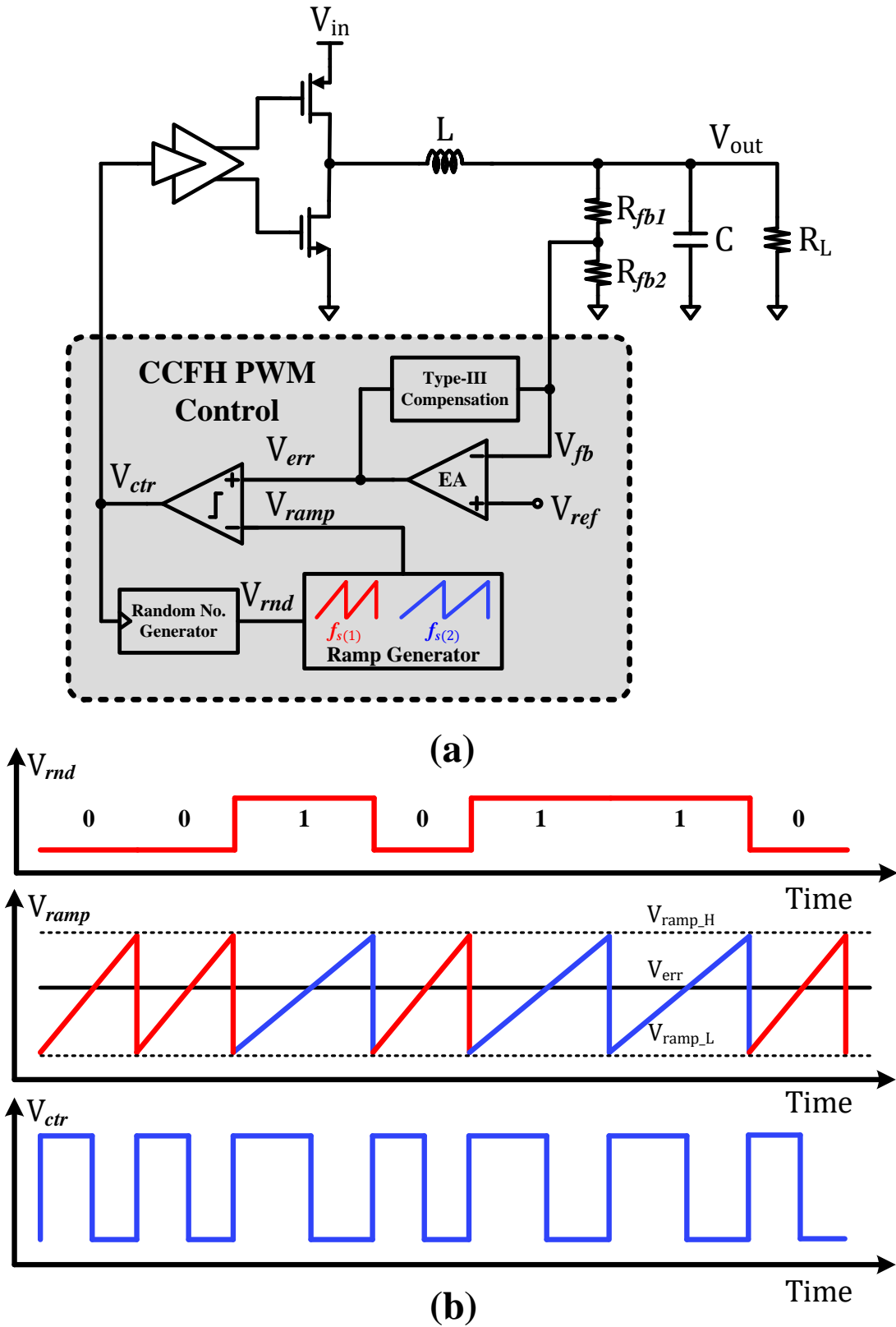


Figure 4.7 Spur-free constant cycle frequency hopping (CCFH) control [36]: (a) Block diagram, and (b) Associated waveforms.

where γ_j is a Fourier series coefficient, $\Delta T = (1/f_{s(2)} - 1/f_{s(1)})$ and k is a running integer that counts the multiples of $(1/f_{s(2)})$ that have elapsed since time zero (at which $f_{s(2)}$ was selected and not $f_{s(1)}$). This reveals that spurious content is modulated by sine and cosine functions that change both polarity and magnitude as the integer k changes over time which enables full spur-elimination. Due to the periodic nature of the modulating functions and assuming that $(f_{s(1)}\Delta T) = (m/n)$ where m, n are two arbitrary integers, k can be assumed to take values from a finite set of integers $[1, 2, \dots, n]$. Thus, spur-elimination condition can be mathematically expressed as [36]:

$$\left(\frac{1}{n}\right) \cdot \sum_{k=1}^n \cos(2\pi j \cdot k \cdot f_{s(1)}\Delta T) = \left(\frac{1}{n}\right) \cdot \sum_{k=1}^n \sin(2\pi j \cdot k \cdot f_{s(1)}\Delta T) = 0 \quad (4.6)$$

In the case where hopping takes place every switching cycle (which was shown to help lower the noise floor peaking), the spur-elimination condition can be stated as [36]:

$$\frac{f_{s(1)}}{f_{s(2)}} = \left(1 + \frac{m}{n}\right) \neq \text{Integer} \quad (4.7)$$

Satisfying this condition eliminates spurious components for all j th harmonics of frequency $f_{s(1)}$ where $(j/n) \neq \text{Integer}$ and frequency $f_{s(2)}$ where $(j/(n+m)) \neq \text{Integer}$. The power of residual spurs for the harmonics of $f_{s(1)}$ at $(j = n, 2n, \dots)$ and of $f_{s(2)}$ at $(j = (n+m), 2(n+m), \dots)$ are typically below the noise floor realizing that γ_j becomes very small for large values of j .

Designing with a set of frequencies $(f_{s(1)}, f_{s(2)}, \dots, f_{s(M)})$ rather than just two helps spreading spurious energy across M bins extending throughout the frequency range $f_{s(M)} - f_{s(1)}$ thus, lowering noise floor peaking [36]. Similar mathematical treatment for the case

where a set of frequencies is used was conducted. Spur elimination for a given frequency $f_{s(i)}$ and its harmonics can be accomplished if the condition in (4.7) holds true between $f_{s(i)}$ and only one other frequency in the set which greatly facilitates practical implementation. Thus, if for a given frequency $f_{s(M)}$ the condition in (4.7) is satisfied relative to all other frequencies in the set, spur-free operation is achieved. This condition can be expressed as [36]:

$$\frac{f_{s(M)}}{f_{s(i)}} = \left(1 + \frac{m_i}{n_i}\right) \neq \text{Integer for } i = 1 \text{ to } M - 1 \quad (4.8)$$

It is worth-while mentioning that spur-free operation relies on the relative ratios between selected design frequencies rather than their absolute values. Moreover, the spur-elimination condition is a low sensitivity one, that is, errors in frequencies ratio can be tolerated as shown in Fig. 4.8 which depicts the normalized fundamental spur magnitude versus the ratio of frequencies for $n = 10$. This is a very important characteristic for a successful practical implementation where non-idealities and mismatches are inevitable. The effectiveness of the described spur-free control in powering noise-sensitive loads was demonstrated by directly powering a GSM power amplifier without the need for post-regulation to work in compliance [6]. Incorporating CCFH control in PWM architecture was rather straight-forward as the designer has direct control over the switching frequency. However, a similar technique was demonstrated in a pulse frequency modulation (PFM) architecture where the switching frequency is indirectly controlled through the design of the ON time [38].

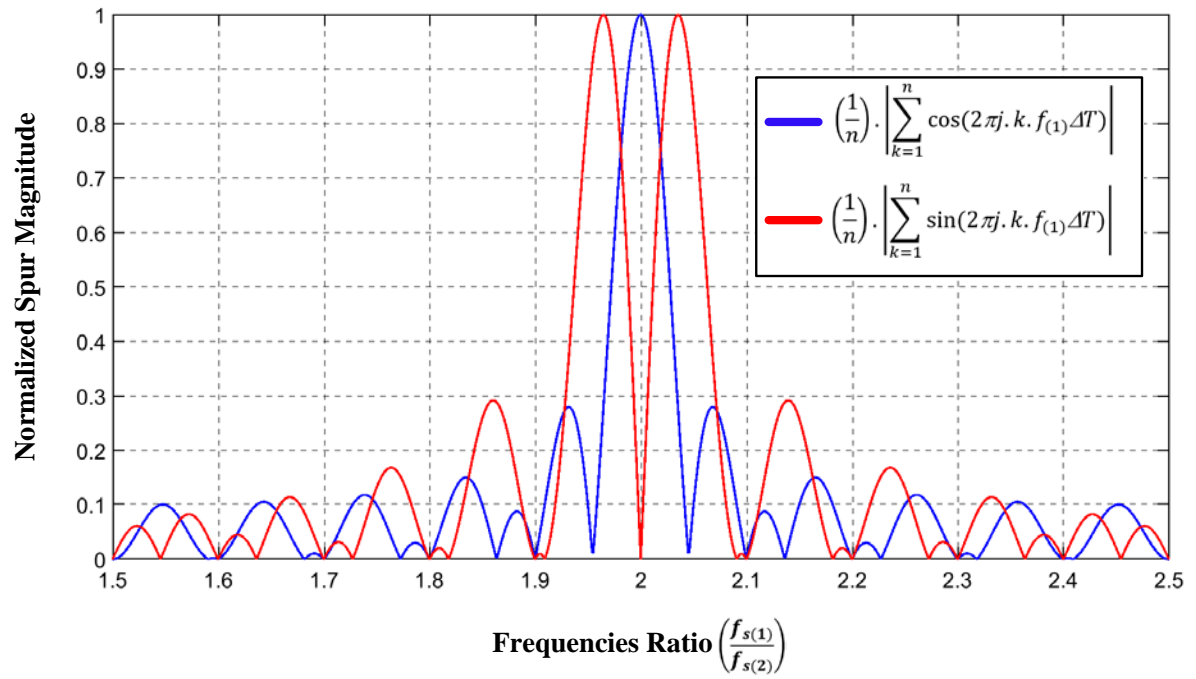


Figure 4.8 Normalized fundamental spur ($j = 1$) magnitude versus the ratio of frequencies for $n = 10$.

CHAPTER 5

PROPOSED SPUR-FREE CURRENT-MODE HYSTERETIC BUCK CONVERTER

Adopting the spur-free CCFH switching described in the previous chapter in PWM controllers is straightforward because of the direct control over the switching frequencies (i.e. the condition in (4.8) can be easily ensured). However, in a self-oscillating hysteretic controller, incorporating such technique is challenging due to the dependency of the switching frequency on the operating conditions. In this thesis, an implementation of a spur-free CCFH hysteretic buck converter is proposed to address these challenges. The remainder of this chapter will discuss the system-level aspects of the proposed design.

5.1 Top-Level Implementation

The top-level block diagram of the proposed current-mode hysteretic buck converter incorporating spur-free CCFH is shown in Fig. 5.1, where the startup module is used to pass the hysteretic controller output or the digital soft-startup output to the power switches in normal or startup conditions respectively. The details of the startup module will be discussed in chapter 6. The high-gain error amplifier (EA) is added to the control loop in order to improve the DC load regulation of the converter by adjusting the average of the feedback voltage (V_{fb}) such that the offset due to the DCR resistance of the inductor is eliminated. In normal operation, the hysteretic band of the comparator is modulated randomly in order to hop the switching frequency of the converter between a set of M frequencies. Although hopping could have been achieved by modulating other parameters, such as the control loop delay, the proposed method is chosen since the hysteretic band can be more accurately controlled. The hysteretic band is modulated every switching cycle by using the rising edge

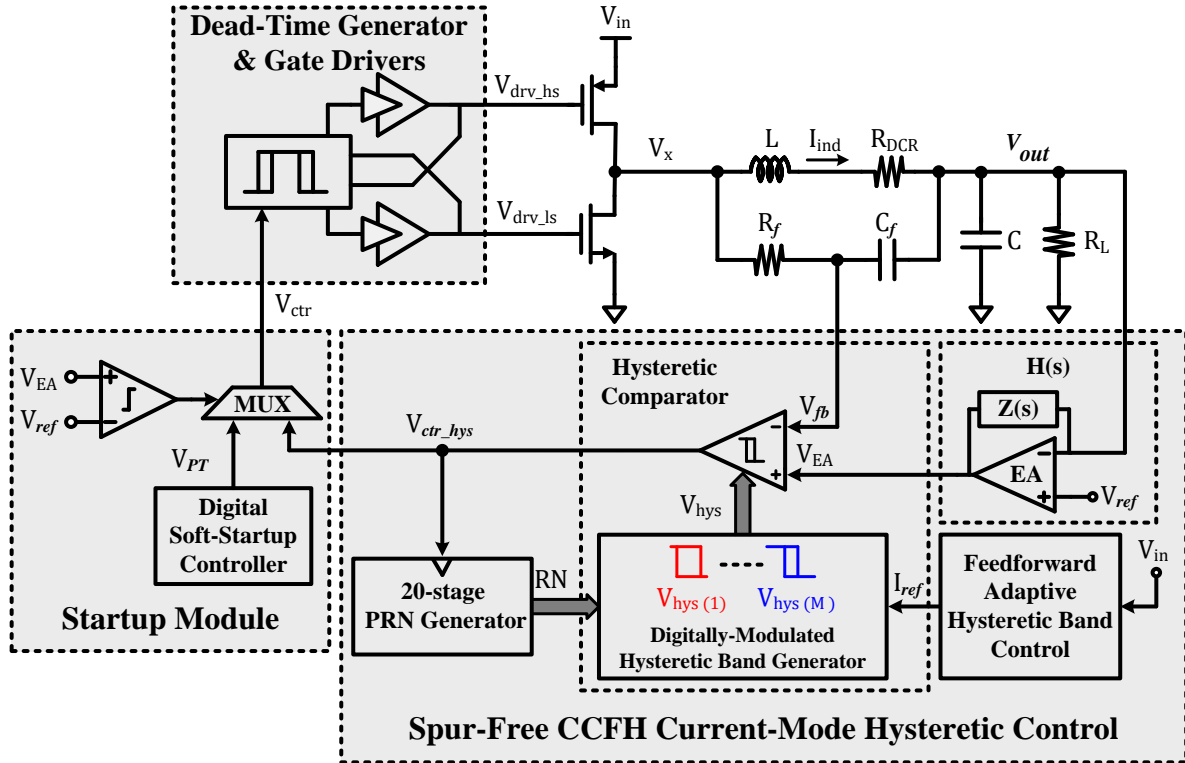


Figure 5.1 Top-level block diagram of the proposed current-mode hysteretic buck converter incorporating spur-free CCFH control.

of the control signal (V_{ctr_hys}) to trigger at 20-stage, digital Pseudo Random Number (PRN) generator, which in turn selects a different hysteretic band. This configuration ensures that modulation takes place only at the end of a full cycle, which eliminates switching duty-cycle disturbances. It also ensures the hysteretic band is modulated every cycle, which results in better spectral spreading due to rapid hopping [36].

5.2 Spur-Free Operation

Although the design in Fig. 5.1 implements the random CCFH component, spur elimination also requires meeting the condition in (4.8), and therefore, the sizes of the hysteretic band cannot be arbitrary. By inspecting the condition in (4.8), an important observation that can be made is the fact that it is relative in nature, i.e. a condition on ratios

rather than on absolute values of frequencies. This essentially implies that variations in the absolute values of the switching frequencies are irrelevant and only the mutual relationship is what matters. This observation can be leveraged in hysteretic controllers where the absolute values of switching frequencies are always operating-conditions-dependent. Using (3.2), the condition in (4.8) can be rewritten as:

$$\frac{f_{s(M)}}{f_{s(i)}} = \frac{\tau_{RC}(V_{hys(i)}/V_{in}) + \tau_D}{\tau_{RC}(V_{hys(M)}/V_{in}) + \tau_D} = \left(1 + \frac{m(i)}{n(i)}\right) \neq \text{Integer, for } i = 1 \text{ to } (M - 1) \quad (5.1)$$

By minimizing the loop delay (τ_D) through careful design of the comparator and the dead-time generator and gate drivers, and maximizing both the current sensing filter's time-constant (τ_{RC}) and hysteretic band sizes, the loop delay can be made substantially smaller than $\tau_{RC}(V_{hys(M)}/V_{in})$, in which case (5.1) can be further simplified as:

$$\frac{f_{s(M)}}{f_{s(i)}} = \frac{V_{hys(i)}}{V_{hys(M)}} = \left(1 + \frac{m(i)}{n(i)}\right) \neq \text{Integer} \quad \text{for } i = 1 \text{ to } (M - 1) \quad (5.2)$$

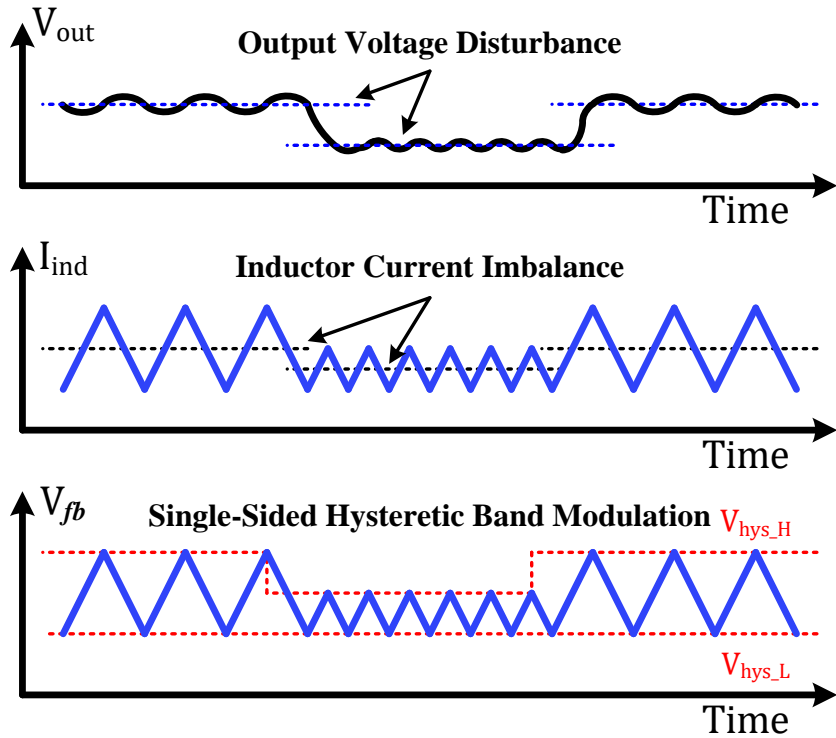
Thus, the condition of spur elimination can be met, irrespective of the absolute band sizes or switching frequencies, by setting the ratios between the hysteretic bands according to (5.2).

5.3 Eliminating Inductor Current Imbalance

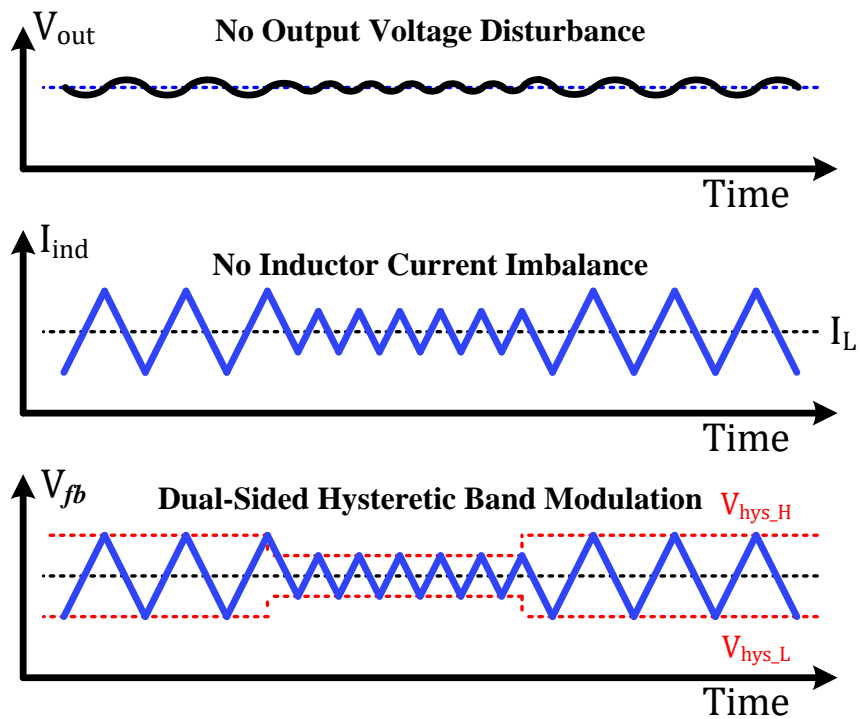
One of the common side effects of employing any form of frequency hopping in switching power converters is inductor current imbalance, i.e. the average inductor current is disturbed due to changing the switching frequency even if the load current is staying constant [40]. In the time domain, this effect manifests itself as additional transients in the output voltage every time the frequency is hopped, which makes meeting the voltage ripple requirements quite difficult. In the frequency domain, it manifests itself as peaking in the

low-frequency noise floor and/or additional low-frequency spurs shaped by the LC output filter [36]. One method to eliminate this problem in PWM-controlled converters is to use equal rising and falling slopes in the ramp signal, i.e. a triangular ramp [33, 41]. Another method relies on injecting an additional pulse into the control signal to ensure that frequency hopping takes place exactly at the point where the inductor current is equal to the load current such that the average of the inductor current is preserved as the frequency is hopped [40]. However, since there is no ramp signal in hysteretic controllers, and injecting an additional pulse at the correct time to preserve constant average inductor current requires complex and precise timing control (difficult to achieve reliably in self-oscillating topologies), alternative methods must be developed for hysteretic controllers.

One method that can be employed for modulating the hysteretic band in a hysteretic controller is referred to as single-sided band modulation, where only one of the bounds of the band is modulated while the other is maintained at a constant level. This is illustrated in Fig. 5.2(a) where the hysteretic band is modulated between only two different values for simplicity by keeping the lower hysteretic bound (V_{hys_L}) constant and modulating the upper bound (V_{hys_H}). As shown in the figure, this method results in inductor current imbalance since the peak current is changing while the valley is not, and thus the average inductor current is changing, which causes output voltage disturbances. In order to eliminate this imbalance, this work proposes a dual-sided band modulation approach, where both the upper and lower bounds of the hysteretic band are modulated simultaneously and symmetrically as illustrated in Fig. 5.2(b), where V_{hys_H} and V_{hys_L} are modulated such that their average is always constant. As shown in the figure, this approach ensures the average inductor current stays constant regardless of the hysteretic band size or the switching frequency. Thus, output



(a)



(b)

Figure 5.2 Key waveforms for: (a) Single-sided hysteretic band modulation, and (b) Dual-sided hysteretic band modulation.

voltage disturbances due to hopping are eliminated and the worst-case output voltage ripple will simply correspond to the lowest switching frequency.

5.4 Reducing Switching Frequency Variations

Although incorporating spur-free CCFH switching in the hysteretic controller eliminates the spurious noise irrespective of variations in the average switching frequency of the converter, excessive variations are still undesired as they can potentially degrade efficiency and result in highly varying output voltage ripple. Using (3.2), and assuming negligible loop delay and equal probability of occurrence for each of the hysteretic bands used for frequency hopping, the average switching frequency $f_{s(avg)}$ can be derived as:

$$f_{s(avg)} = \frac{M}{\sum_{i=1}^{i=M} \left(\frac{1}{f_{s(i)}} \right)} = \frac{M V_{in} D (1 - D)}{\tau_{RC} \sum_{i=1}^{i=M} V_{hys(i)}} \quad (5.3)$$

which shows that $f_{s(avg)}$ is a strong function of the input voltage V_{in} . To reduce variability in $f_{s(avg)}$, this work proposes employing feedforward adaptive hysteretic band control as shown in Fig. 5.1, to adapt the digitally-modulated hysteretic bands such that $(V_{hys(i)}/V_{in})$ for $i = 1$ to M is kept constant. With such design, although the average switching frequency continues to vary with the duty-cycle and the sensing filter time-constant, but the overall variations are greatly reduced.

5.5 Loop Stability and Compensation

The proposed top-level implementation contains a ripple-based, fast current regulation loop, and an average-based, high-gain voltage regulation loop. To ensure the stability of the voltage regulation loop, its transfer function must be obtained to determine the needed compensation, i.e. $H(s)$. The control-to-output transfer function of the voltage

regulation loop is $V_{out}(s)/V_{EA}(s)$, and it can be derived by observing that the current regulation loop sets the average of $V_{EA}(s)$ and the feedback signal ($V_{fb}(s)$) to be equal [42]. Considering that $V_{fb}(s)$ can be expressed in terms of inductor current ($I_{ind}(s)$) and output voltage ($V_{out}(s)$), $V_{EA}(s)$ can be written as:

$$V_{EA}(s) = \left(\frac{1 + s \frac{L}{R_{DCR}}}{1 + s R_f C_f} \right) R_{DCR} I_{ind}(s) + V_{out}(s) \quad (5.3)$$

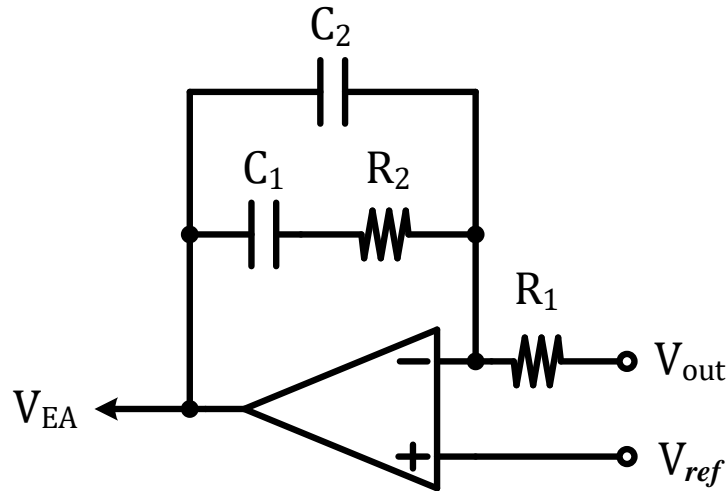
where L is the inductor and R_{DCR} is its series resistance. By expressing the inductor current in terms of the load resistance (R_L) and output capacitor (C), $V_{out}(s)/V_{EA}(s)$ can be expressed as:

$$\frac{V_{out}(s)}{V_{EA}(s)} = \left(\frac{R_L}{R_L + R_{DCR}} \right) \left(\frac{1 + s R_f C_f}{1 + s \frac{R_L R_f C_f + L + R_L R_{DCR} C}{R_{DCR} + R_L} + s^2 \frac{R_L L C}{R_{DCR} + R_L}} \right) \quad (5.4)$$

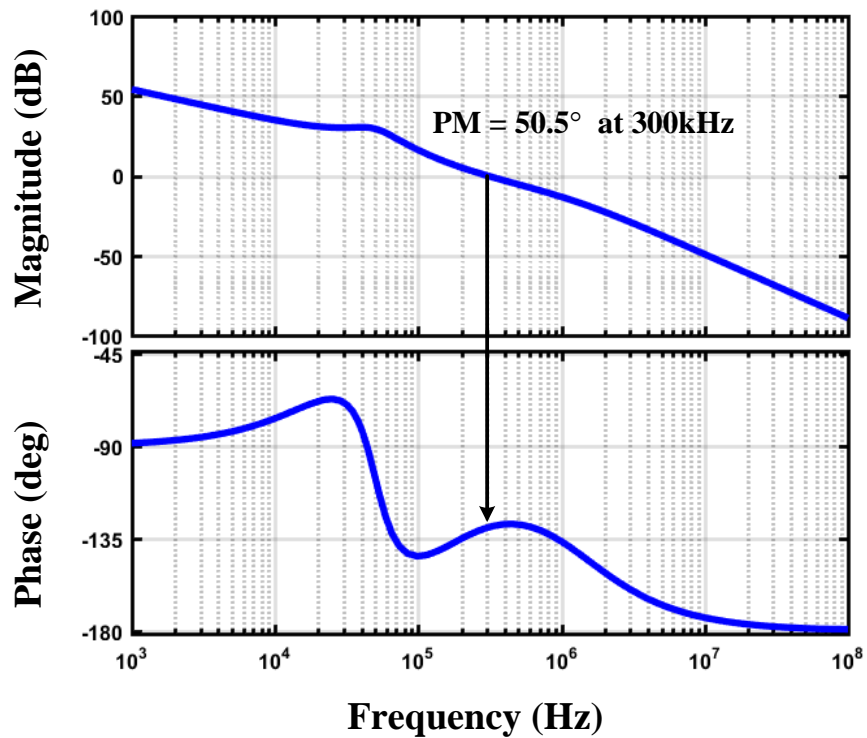
Since R_{DCR} and C_f are typically small, this transfer function contains two complex poles at approximately $(1/\sqrt{LC})$. Thus, the compensation network $H(s)$ in Fig. 5.1 can be type-I, type-II, or type-III to ensure the stability of the loop. However, considering that (5.4) contains a zero at $(1/R_f C_f)$, which facilitates compensation, a fully integrated type-II network is chosen to avoid the excessively slow response and large off-chip capacitor of a type-I network, and the large number of passives of a type-III network [2]. In this case, $H(s)$ can be represented as:

$$H(s) = \frac{(1 + s R_2 C_1)}{s R_1 (C_1 + C_2) \left(1 + s \left(\frac{C_1 C_2}{C_1 + C_2} \right) R_2 \right)} \quad (5.5)$$

which can be implemented as shown in Fig. 5.3(a), and results in the overall voltage loop gain and phase responses shown in Fig. 5.3(b).



(a)



(b)

Figure 5.3 Type-II compensation network: (a) Circuit realization, and (b) Loop gain and phase responses.

CHAPTER 6

PROPOSED CIRCUIT-LEVEL REALIZATION AND MEASUREMENT

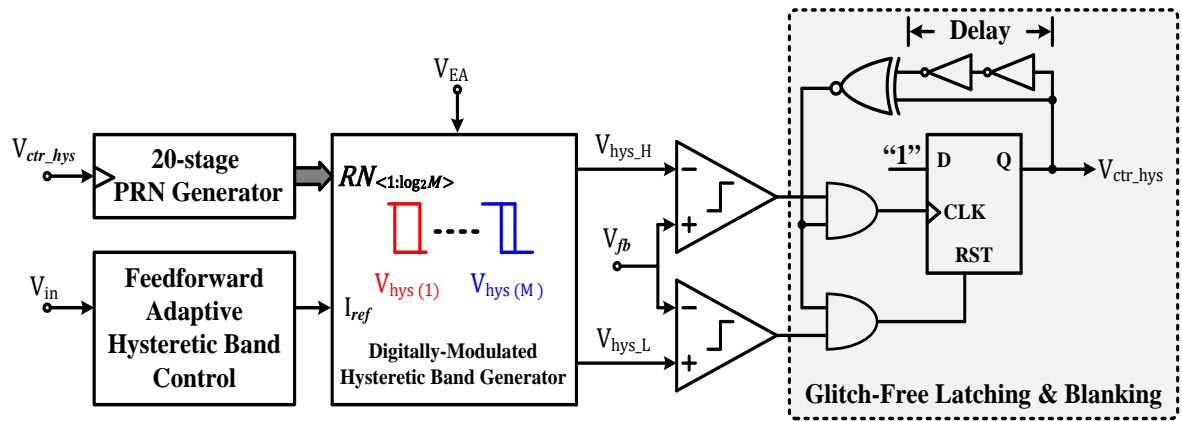
RESULTS

6.1 Circuit-Level Realization

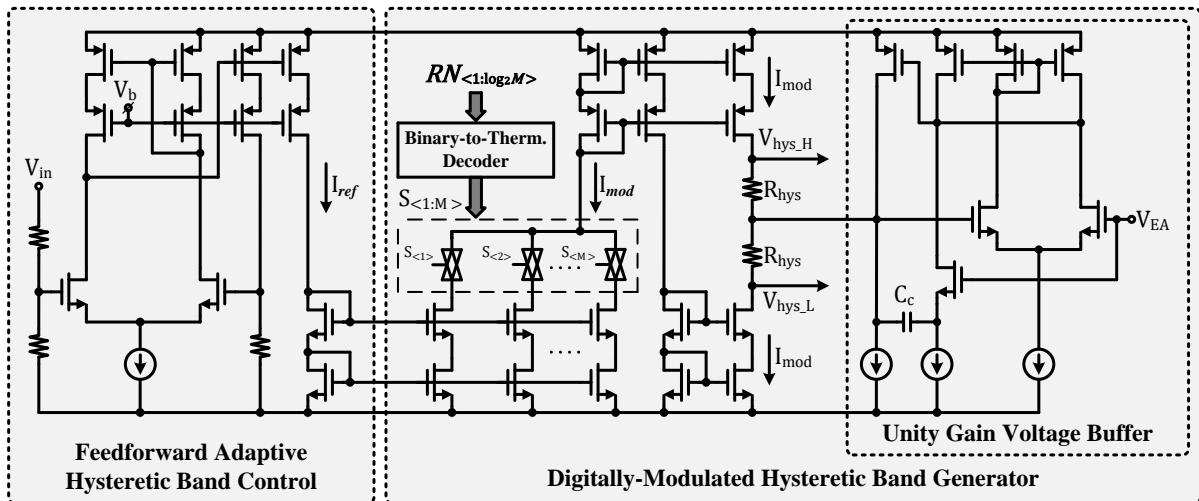
The circuit-level realization of the critical blocks in the proposed spur-free CCFH current-mode hysteretic buck converter will be presented.

6.1.1 The Spur-Free CCFH Hysteretic Controller

The dual-sided hysteretic function needed for the proposed spur-free CCFH controller is realized using two independent comparators with the hysteretic bounds generated separately using a band generator as shown in Fig. 6.1(a). The circuit realization of the digitally-modulated hysteretic band generator is shown in Fig. 6.1(b). Since the feedback signal (V_{fb}) used by the comparators is derived from the rather noisy switching node, it can falsely trigger the comparators, and thus, a glitch-free latching circuit is implemented using an XNOR gate and delay cells to provide a blanking period for latching the comparators' outputs [43]. Moreover, to minimize the control loop delay, the comparators are carefully implemented to minimize their input referred offset and maximize their speed using a multi-stage design as shown in Fig. 6.2. A unity-gain voltage buffer is used to set the middle point between the identical resistors (R_{hys}) to the same level as the error signal (V_{EA}) of the error amplifier, such that the upper and lower hysteretic bounds (V_{hys_H} and V_{hys_L}) are generated symmetrically around V_{EA} by forcing the modulation current (I_{mod}) into the two resistors. This configuration implements the feedback path of the voltage regulation loop shown in Fig. 5.1. To modulate the hysteretic band, I_{mod} is generated through an M -branches of current



(a)



(b)

Figure 6.1 The proposed spur-free CCFH hysteretic controller: (a) Simplified schematic showing the glitch-free latching circuit, and (b) Transistor-level details of the hysteretic band generator with feedforward adaptive control.

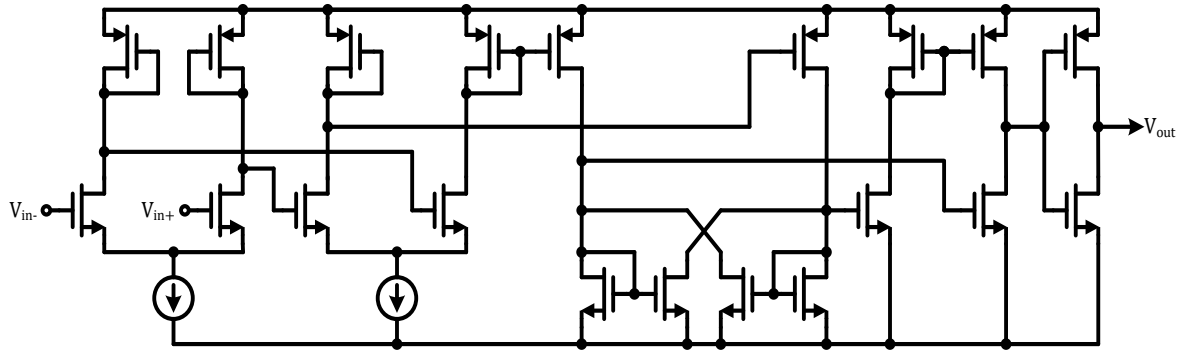


Figure 6.2 High-speed, low-offset comparator realization.

mirrors from the shared reference current (I_{ref}), where I_{mod} is modulated by enabling/disabling branches using a 20-stage ($\log_2 M$)-bit PRN generator followed by a binary-to-thermometer decoder. Thermometer coding is selected to guarantee the monotonicity of the generated bands and to eliminate glitches that occur with standard binary coding. The finger ratios between the current mirror branches are designed to meet the spur-elimination condition in (5.2). The adaptation of the hysteretic band with the input voltage is implemented using the feedforward adaptive hysteretic band controller shown in Fig. 6.1(b), where a potential divider from the input voltage and a voltage-to-current converter are used together to modulate the reference current (I_{ref}) as a function of the input voltage. This way, adaptation with the input voltage can be achieved while preserving the spur-elimination condition in (5.2) since I_{ref} is common to all values of I_{mod} . The schematic of the type-II compensated error amplifier is shown in Fig. 6.3.

The 20-stage ($\log_2 M$)-bit PRN generator is implemented using the Linear Feedback Shift Register (LFSR) shown in Fig. 6.4, where 20 D flip-flops are used with an XNOR gate to generate a 20-bit pseudo random digital code. Therefore, if the desired number of hysteretic bands is M , only $\log_2 M$ bits are needed out of the 20 bits generated. Although any

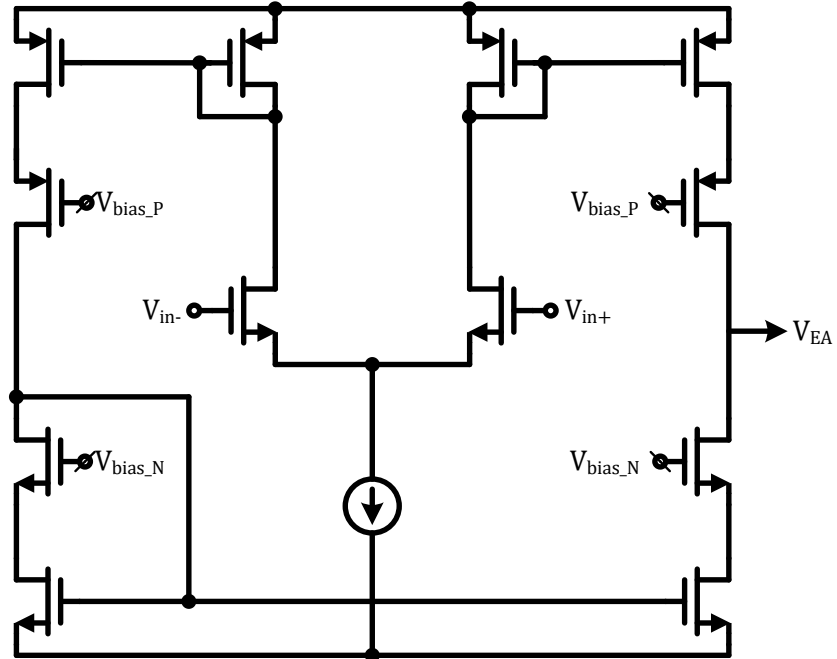


Figure 6.3 Error amplifier circuit-level realization.

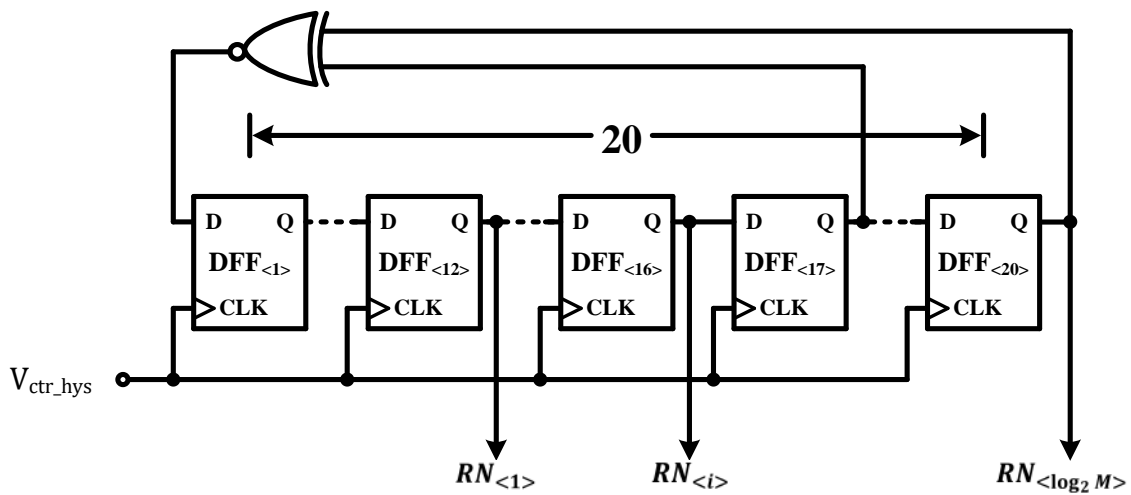


Figure 6.4 Pseudo Random Number (PRN) generator using a 20-stage Linear Feedback Shift Register (LFSR).

bits can be selected, it is important to note that selecting consecutive bits should be avoided since in that case, and for any given code, the number of possible outcomes for the next code would be less than the theoretical number (i.e. M). This introduces a memory effect that degrades the randomness of the generated codes. Instead, the $\log_2 M$ bits should be tapped from non-consecutive flip-flops such that for any code, there is an equal likelihood for the next code to be any of the M possibilities independent of the current code, thereby eliminating memory effects.

6.1.2 All-Digital Soft-Startup

During startup conditions, the main control loop detects that the output voltage is far off from the target value, and generates a large error signal. If no additional precautions are taken, this large error signal produces excessively long ON-time intervals, which leads to dangerously high in-rush current [44]. To mitigate this issue, the main controller is commonly bypassed during startup conditions, and a separate soft-startup controller is employed instead to control the in-rush current. Once the output reaches its target value, control is handed off from the soft-startup to the main control loop for normal operation. A conventional soft-startup circuit is shown in Fig. 6.5, where the sawtooth signal (V_{saw}) is compared to a slow ramp voltage (V_{ramp}) to generate a train of pulses with small, yet gradually increasing duty-cycle to control the power switches and the inrush current [44]. However, the generation of the slow ramp requires either an off-chip capacitor and a dedicated pin, or a relatively large on-chip capacitor. Although alternative soft-startup circuits have been proposed to reduce the size of the required on-chip capacitor, their operation remains analog in nature and requires custom circuit design [45].

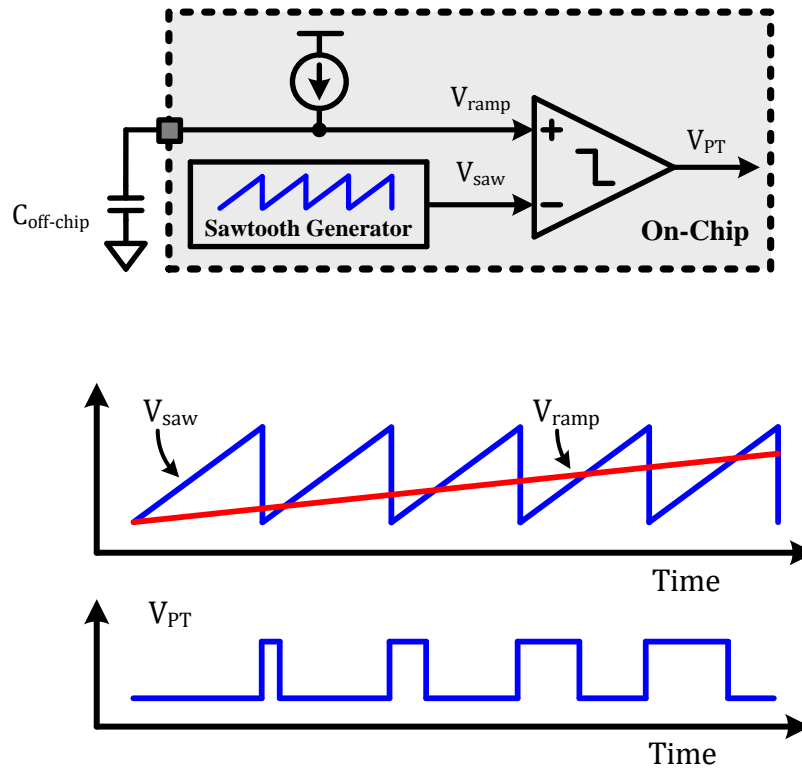


Figure 6.5 Conventional analog realization of a soft-startup circuit and its timing diagrams.

In this work, the all-digital soft-startup circuit shown in Fig. 6.6 with its timing diagrams is proposed. The fundamental idea lies in generating a train of pulses with incremental, digitally-controlled duty-cycle. First, a simple N -stage ring oscillator is implemented to generate N equally-spaced clock phases ($P_{<0>}$ to $P_{<N-1>}$). By combining the rising and falling edges of the various phases using a phase combiner logic circuit, pulses with duty-cycle that is an integer multiple of $(1/2N)\%$ can be generated up to $(2N - 1)/2N \%$. The duty-cycle of the pulses is swept from the minimum to the maximum, with the number of pulses at each duty-cycle controlled using a k -bit counter as shown in Fig. 6.6. In this particular design, a 17-stage ring oscillator is used to generate pulses with duty-cycle that is an integer multiple of 2.94% up to 97.05%, and each duty-cycle is applied for 32

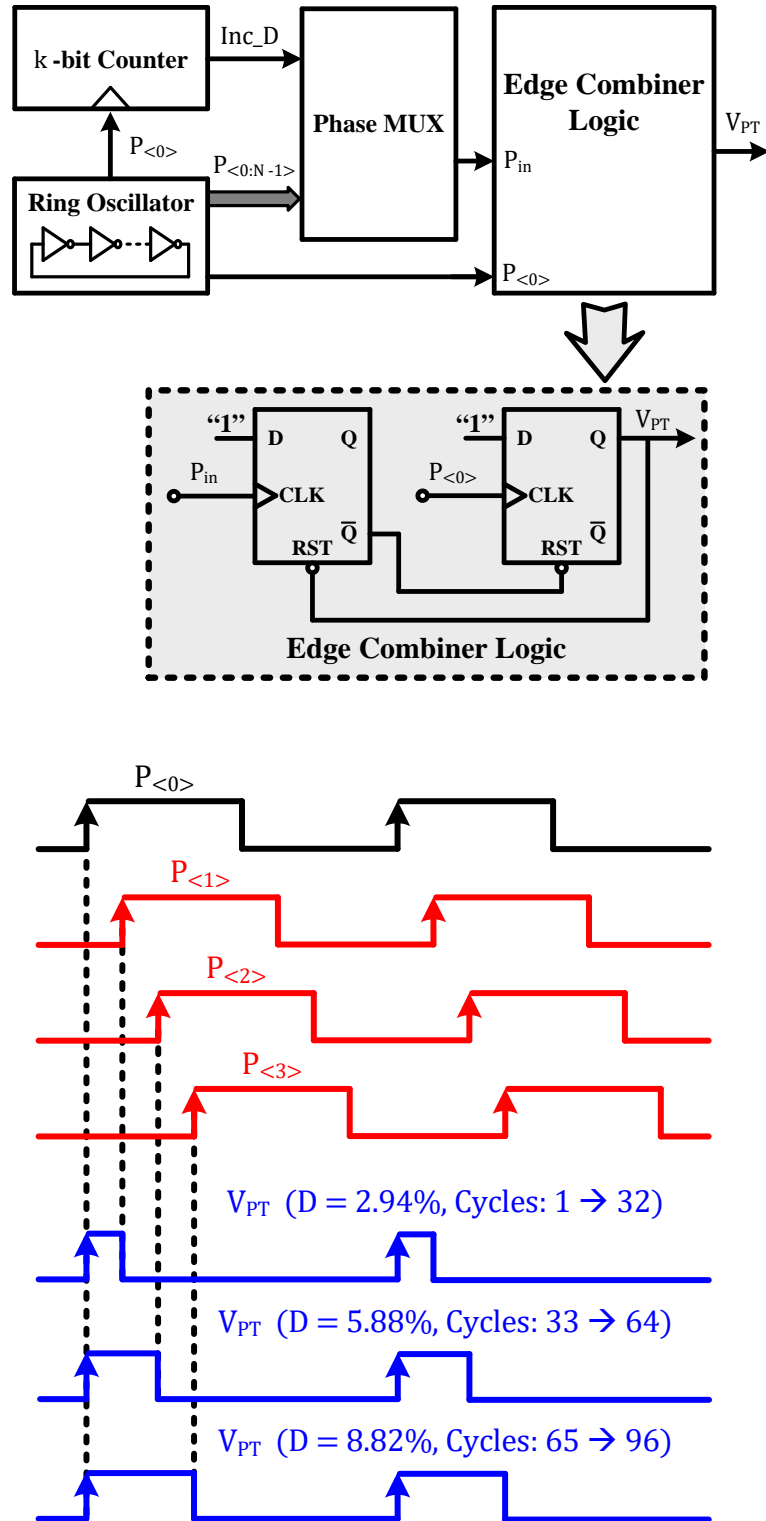
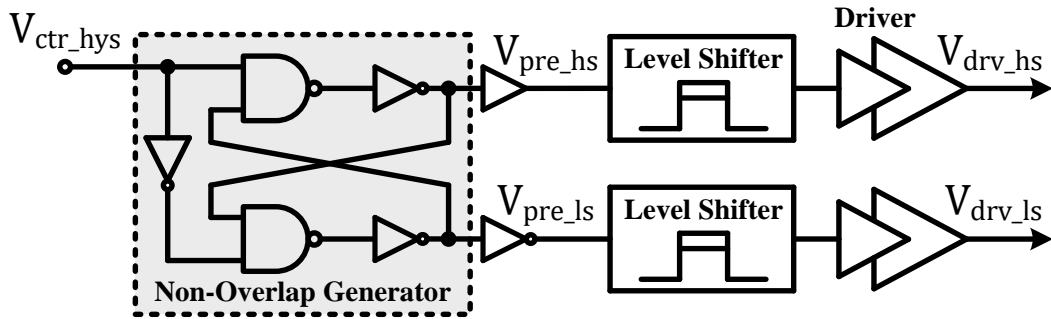


Figure 6.6 Proposed all-digital soft-startup circuit and its timing diagrams.

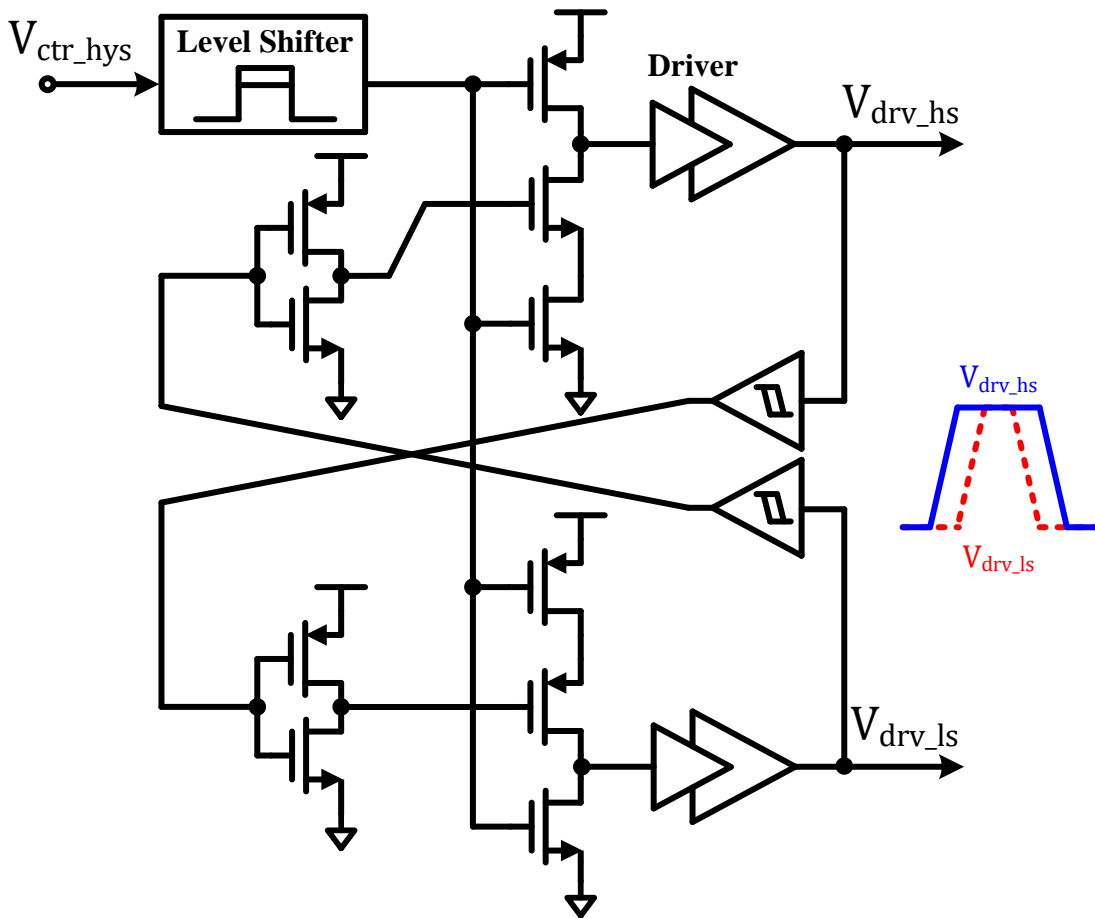
pulses. Once the output of the error amplifier (V_{EA}) exceeds the reference voltage (V_{ref}), the control is handed over to the hysteretic controller of the converter as shown in Fig. 5.1. The proposed all-digital soft-startup can be synthesized using standard digital cells (including the ring oscillator) and requires no analog components, while the soft-startup time can be fine-tuned by changing the k -bit counter size.

6.1.3 Dead-Time Generator and Gate-Drivers

In buck converters, a dead-time must be inserted between the gate control signals of the high-side and low-side power switches to avoid shoot-through current. A standard technique to accomplish that is shown in Fig. 6.7(a), where a non-overlapping clock generator circuit [46] is used to create two versions of the control signal (i.e. V_{pre_hs} and V_{pre_ls}) with a dead-time equal to the total delay of the circuit. However, in order to ensure that the actual dead-time at the gates of the power switches (i.e. V_{drv_hs} and V_{drv_ls}) is always non-zero, the delay mismatches between the level shifters and the gate drivers must be accounted for by making the dead-time, and consequently the loop delay, excessively long. Moreover, the loop delay is further increased due to the additional delay of the level shifters and the gate-drivers. Since the loop delay in the proposed spur-free CCFH hysteretic controller must be minimized to make the condition in (5.2) valid, a different approach is needed. Thus, the dead-time generator circuit in [47] is adopted as shown in Fig. 6.7(b), where the control signal (V_{ctr_hys}) is first level-shifted, and then the gate-drivers are incorporated within the dead-time generation process. The first advantage of such circuit is that the dead-time is inserted right in the gate-drive signals, and thus can be ensured to be non-zero regardless of delay mismatches and without designing the dead-time to be excessively long. The second advantage is that the delay of the gate-drivers becomes part of



(a)



(b)

Figure 6.7 (a) Standard dead-time generator and gate drivers, and (b) Adopted architecture from [47] modified by adding Schmitt triggers to prevent glitches and false triggering.

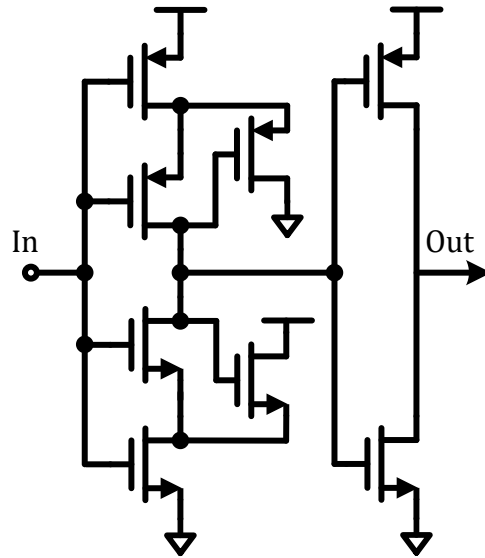


Figure 6.8 Circuit-level realization of the Schmitt trigger.

the dead-time generation, and thus, the number of delay stages needed for generating the dead-time is reduced. These two advantages ultimately result in a much shorter overall loop delay. However, a proposed modification to the circuit in [47] is the additional Schmitt triggers shown in Fig. 6.8. Since the feedback signals of the dead-time generator circuit are now driven by the gate-driver signals, which are noisy, non-monotonic, and have a relatively slow rise and fall times. The Schmitt triggers ensure proper buffering of these signals to prevent glitches and false triggering.

6.2 Measurement Results

The proposed spur-free CCFH current-mode hysteretic buck converter is implemented in a 0.35- μm standard CMOS technology. The converter is designed to operate from Li-Ion battery input levels (i.e. 2.7-4.2 V) and to generate a programmable output in the range of 1.2-1.8 V with a maximum load current of 600 mA. The die photo of the converter is shown in Fig. 6.9 with the main design components highlighted. The total active silicon area of the converter is 0.9 mm^2 , 37% of which is taken by the power switches and their

- (1) High-side switch (PMOS)
- (2) Low-side switch (NMOS)
- (3) Dead-Time Gen. + Gate Drivers
- (4) PRN Generator
- (5) Comparators + Logic
- (6) RC Filter
- (7) Hysteretic Band Generator
- (8) Error Amp. + Type-II Network
- (9) All-Digital Soft-Startup
- (10) Adaptive Feedforward Control
- (11) Biasing
- (12) Analog-Soft Start-up (for testing)
- (13) Decoupling Capacitors

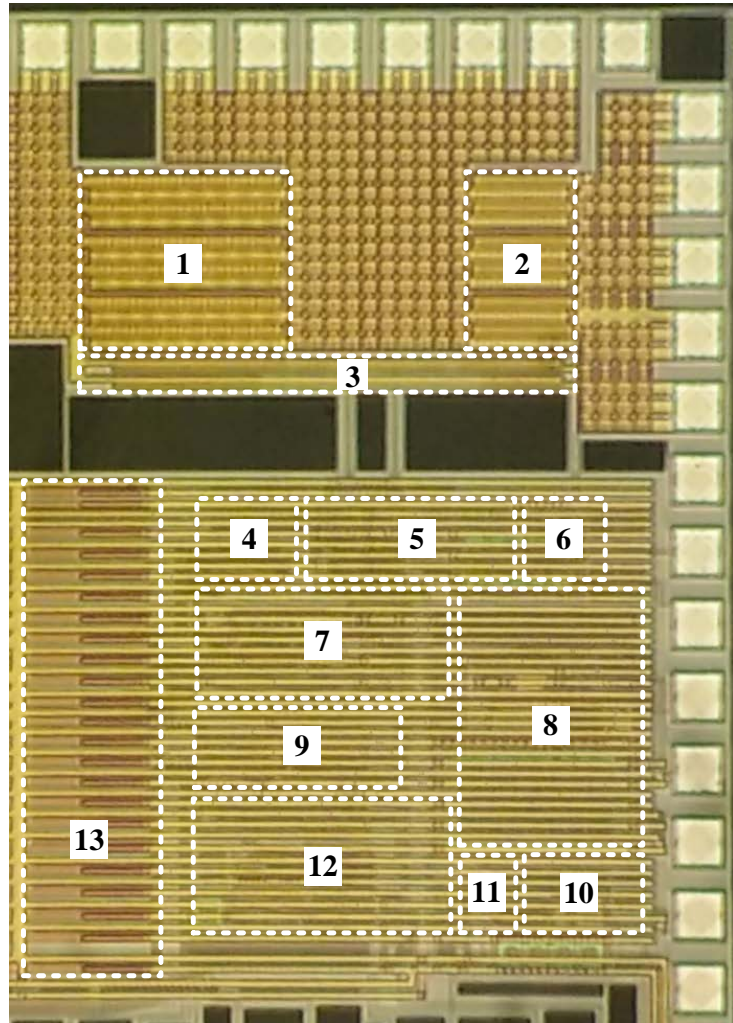


Figure 6.9 Die photo of the proposed spur-free CCFH current-mode hysteretic buck converter with the main building blocks highlighted.

drivers, while the rest is taken by the controller, including the proposed all-digital soft-startup circuit and type-II compensation. The test setup used to characterize the converter is shown in Fig. 6.10, while the evaluation Printed Circuit Board (PCB) is shown in Fig. 6.11 with its main components highlighted. The hysteretic band is hopped between eight different sizes within the following set:

$$V_{hys(i)} = \left(\frac{i+5}{13}\right) \times V_{hys(8)} \quad \text{for } i = 1 \text{ to } 8 \quad (6.1)$$

where $V_{hys(8)}$ is the largest band. This ensures meeting the spur-elimination condition in (5.2).

The measured output voltage spectrum up to 20 MHz under two different operating conditions is shown in Fig. 6.12 and Fig. 6.13 with and without the proposed spur-free CCFH switching technique and with the actual switching frequencies noted. As shown, spurs are fully eliminated as predicted by the theory irrespective of the operating conditions or the actual switching frequencies. The full spreading of the fundamental spur is manifested as a peaking in the noise floor around the average of the switching frequencies used for hopping, while the high-frequency noise floor is barely changed since the energy contained in the higher frequency spurs is much smaller than the fundamental. To demonstrate the importance of meeting the spur-elimination condition in (5.2), the converter is designed to have the option to apply CCFH with two different hysteretic band sizes that violate the condition in (5.2) and the resulting output spectrum is shown in Fig. 6.14, along with the case where the two band sizes are meeting the condition. As shown, when the condition is violated, spurs persist in the output spectrum. Therefore, CCFH by itself is insufficient for eliminating the spurs (will only reduce the spurs as in [34]), and meeting the condition in (5.2) is necessary for eliminating the spurs [36].

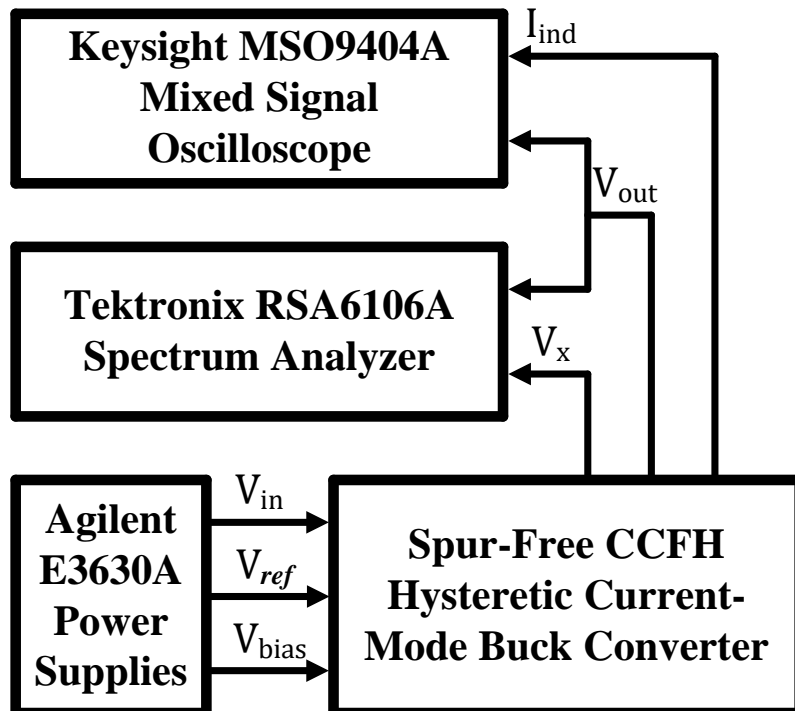
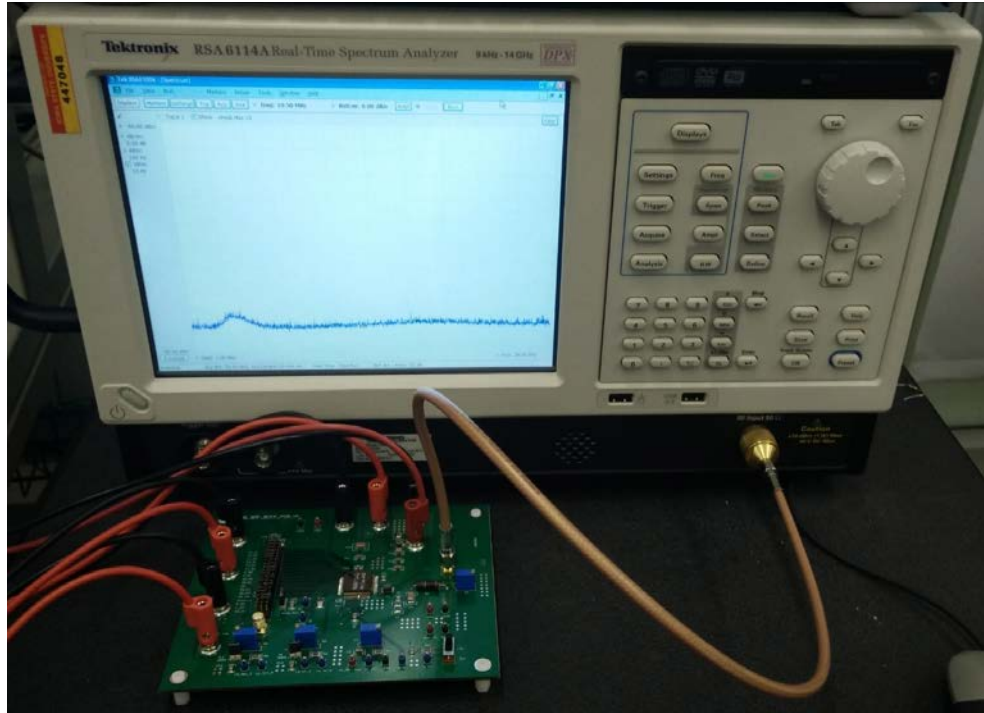


Figure 6.10 Test setup used to characterize the proposed converter.

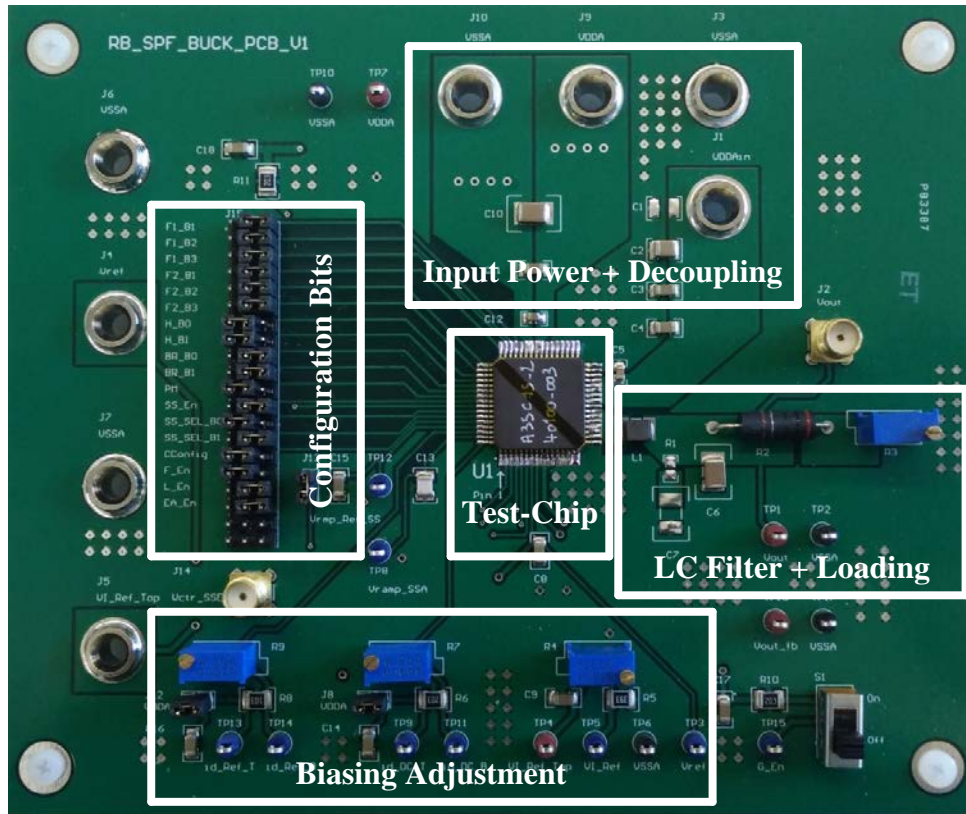
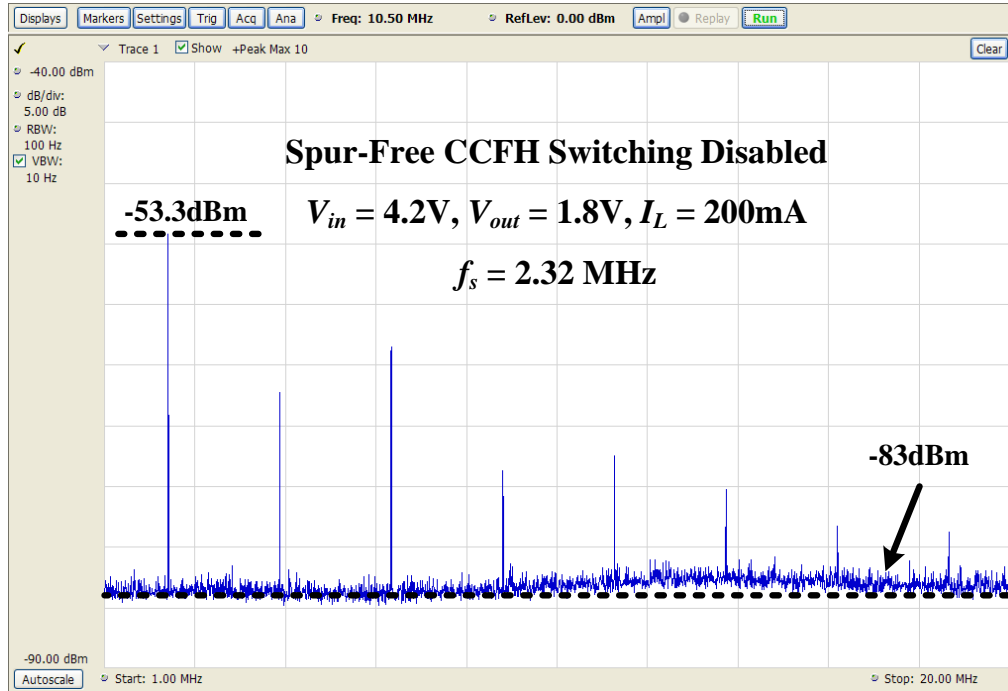
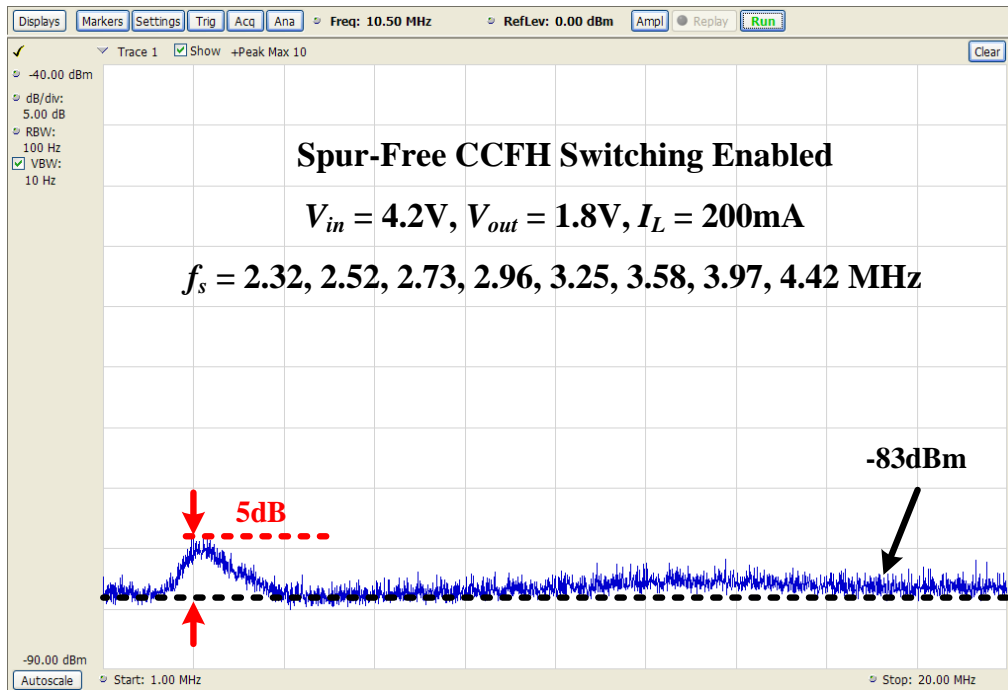


Figure 6.11 Evaluation Printed Circuit Board (PCB) with its main components highlighted.

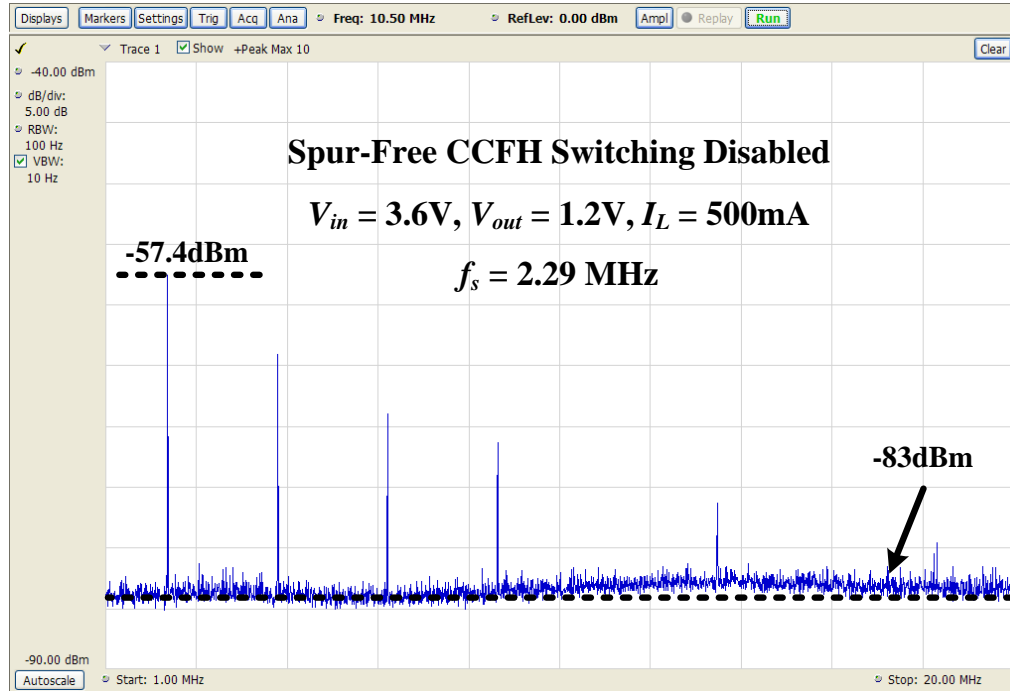


(a)

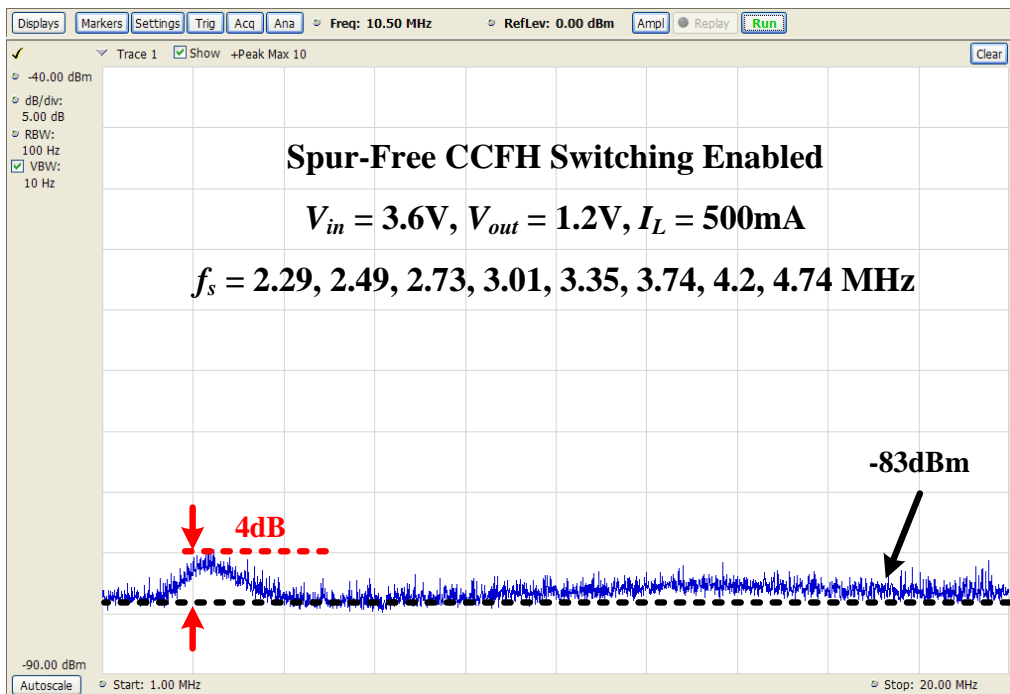


(b)

Figure 6.12 Output voltage spectrum with spur-free CCFH disabled (i.e. single switching frequency) and with the proposed spur-free CCFH switching enabled. Input voltage 4.2 V, output voltage 1.8 V, load current 200 mA.

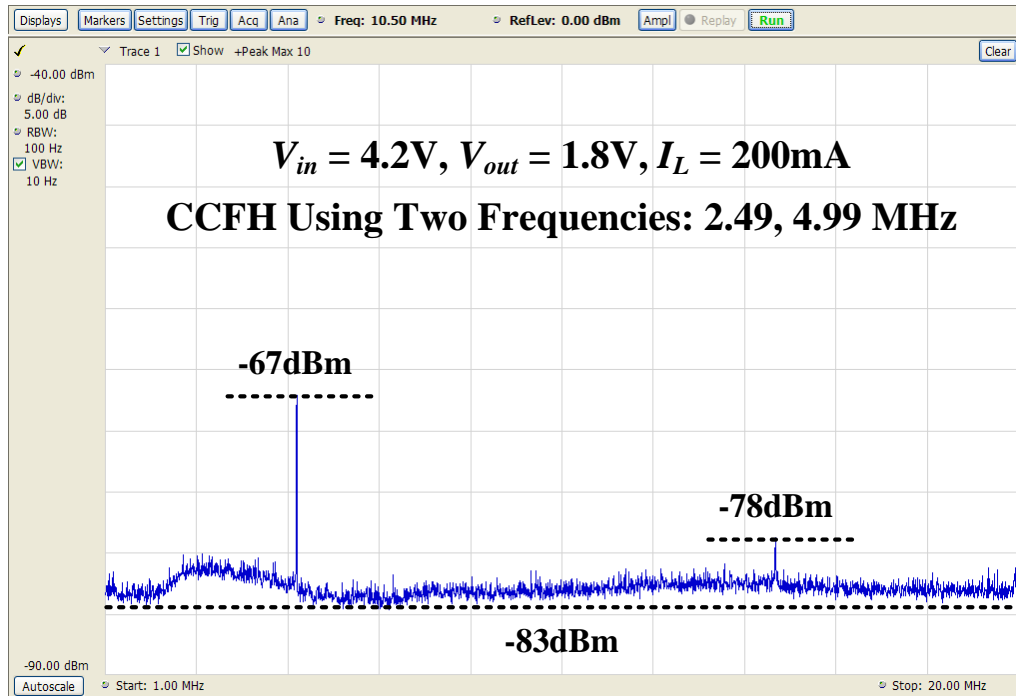


(a)

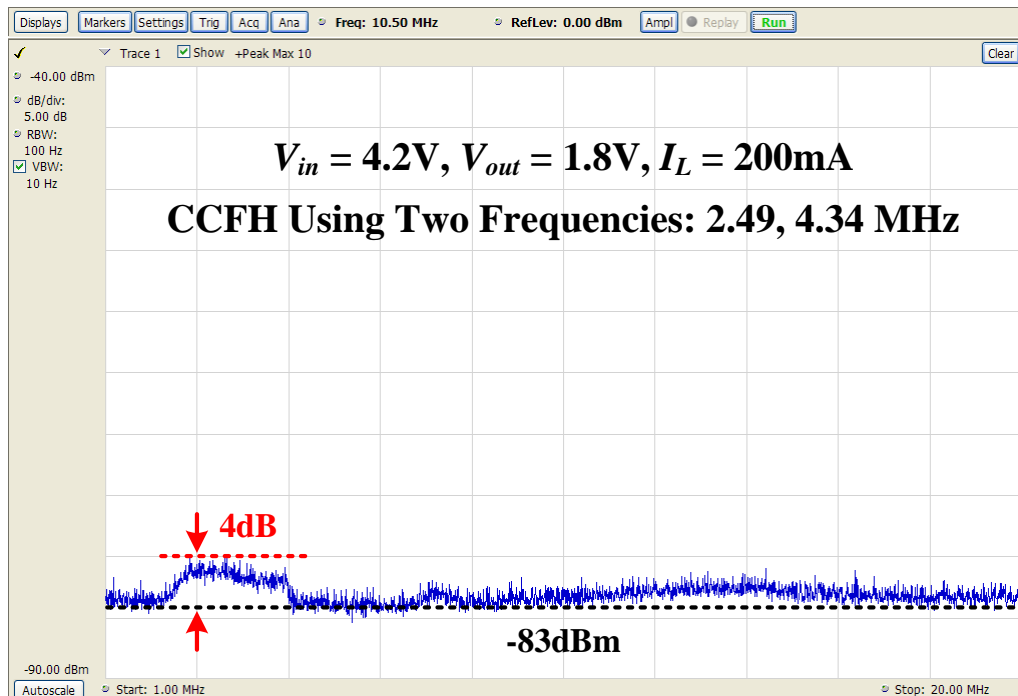


(b)

Figure 6.13 Output voltage spectrum with spur-free CCFH disabled (i.e. single switching frequency) and with the proposed spur-free CCFH switching enabled. Input voltage 6.3 V, output voltage 1.2 V, load current 500 mA.



(a)

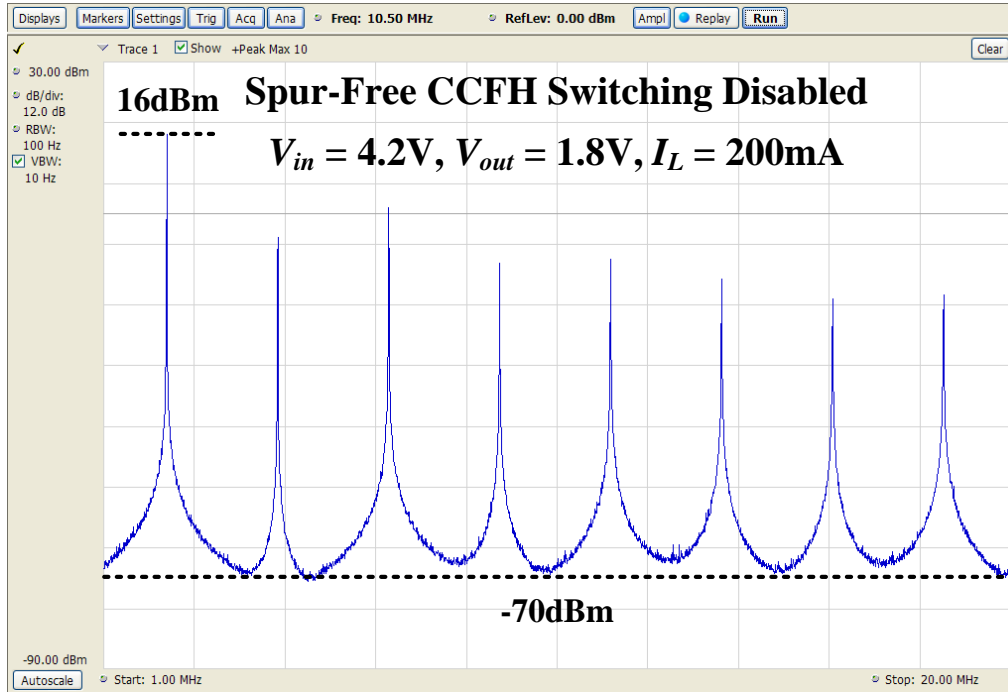


(b)

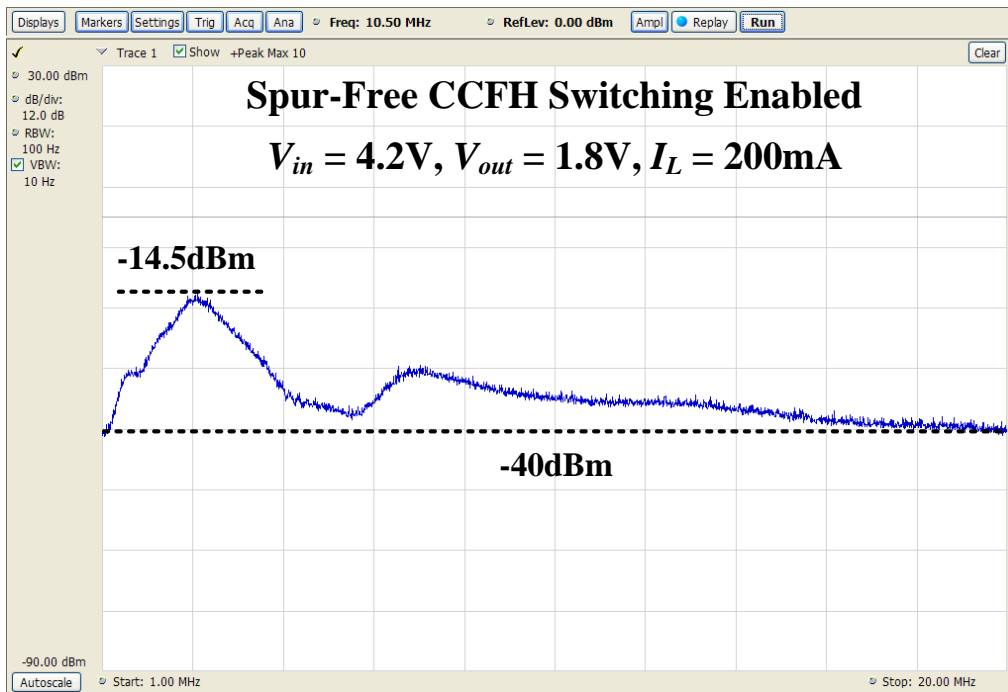
Figure 6.14 Output voltage spectrum with: (a) CCFH between two frequencies that do not meet the spur-elimination condition, and (b) Spur-free CCFH between two frequencies that meet the spur-elimination condition. Operating conditions are noted on each figure.

To demonstrate that full spur elimination is achieved at various nodes within the converter and not just at the heavily-filtered output node, the spectrum is measured at the switching node (the worst in terms of noise). The results are shown in Fig. 6.15 with and without the proposed spur-free CCFH switching, where spurs are fully eliminated. It is worth noting that the ~ 30 dB elevation in the noise floor is due to the large magnitude of the unfiltered spurs at the switching node. The spectrum measurements show that the proposed spur-free hysteretic converter can be used to power noise-sensitive loads, or be integrated within noise-sensitive systems while accommodating widely varying operating conditions with no need for frequency regulation loops to set the location of the spurs accurately.

To validate the effectiveness of the proposed dual-sided hysteretic band modulation in terms of eliminating inductor current imbalance due to hopping, the converter is designed with the option to apply single-sided modulation for comparison purposes. The output voltage is examined without any modulation, and with single- and dual-sided modulation, and the results are shown in Fig. 6.16, Fig. 6.17 and Fig. 6.18 in both the time and frequency domains. As shown, dual-sided modulation is quite effective in minimizing inductor current imbalance, which is evident by observing the reduction in the output transients and their corresponding low-frequency spectrum compared to single-sided modulation. In fact, by comparing Fig. 6.16 and 6.18, dual-sided modulation produces very similar results to the case without any modulation at all in terms of voltage ripple and low-frequency spectral content, while single-sided modulation increases the ripple by over a factor of two and causes about 12 dB peaking in the low-frequency noise floor.

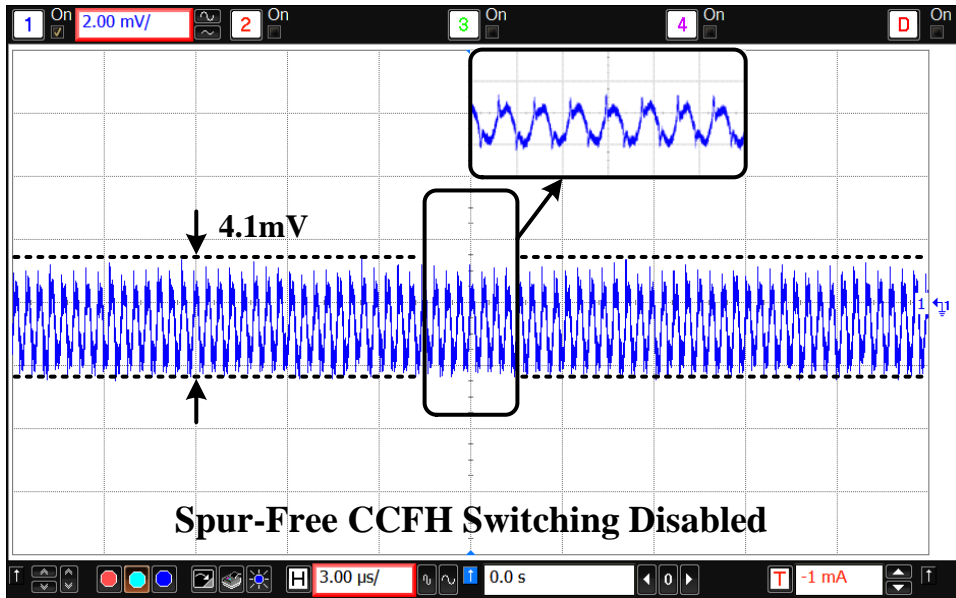


(a)

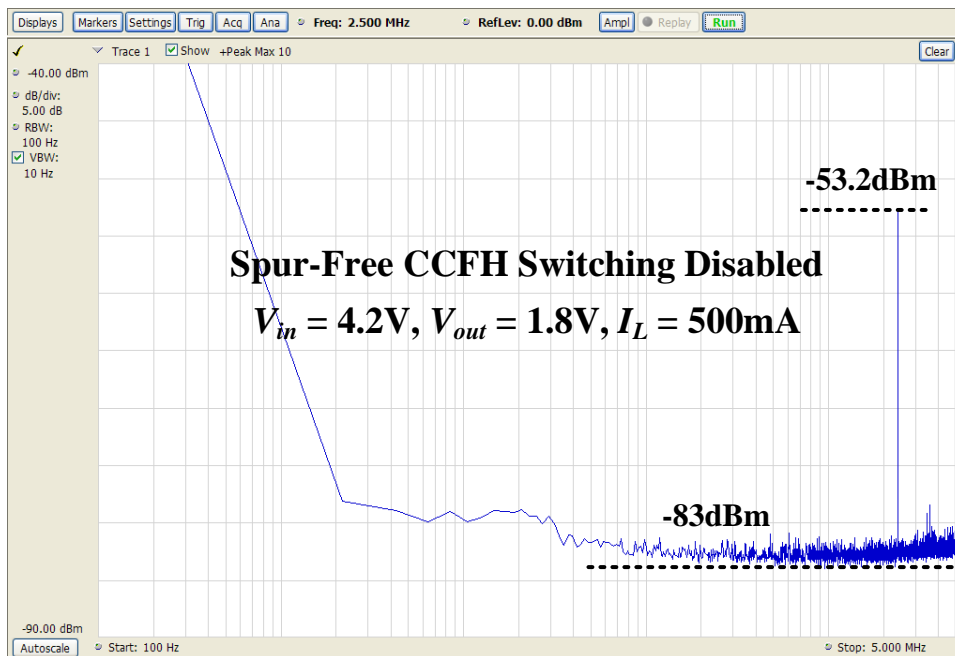


(b)

Figure 6.15 Switching node spectrum with: (a) Spur-free CCFH switching disabled (i.e. single switching frequency), and (b) Spur-free CCFH switching enabled.

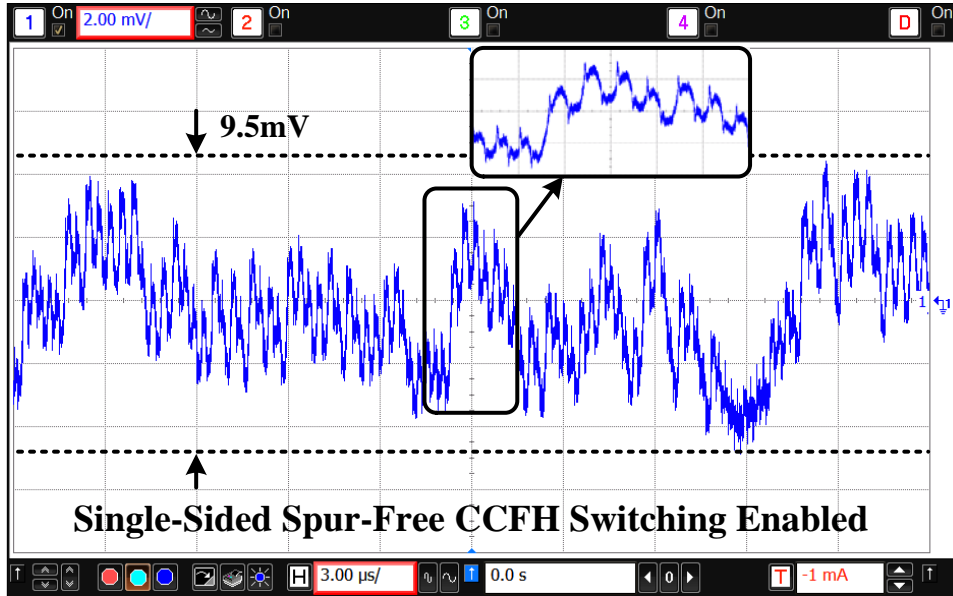


(a)

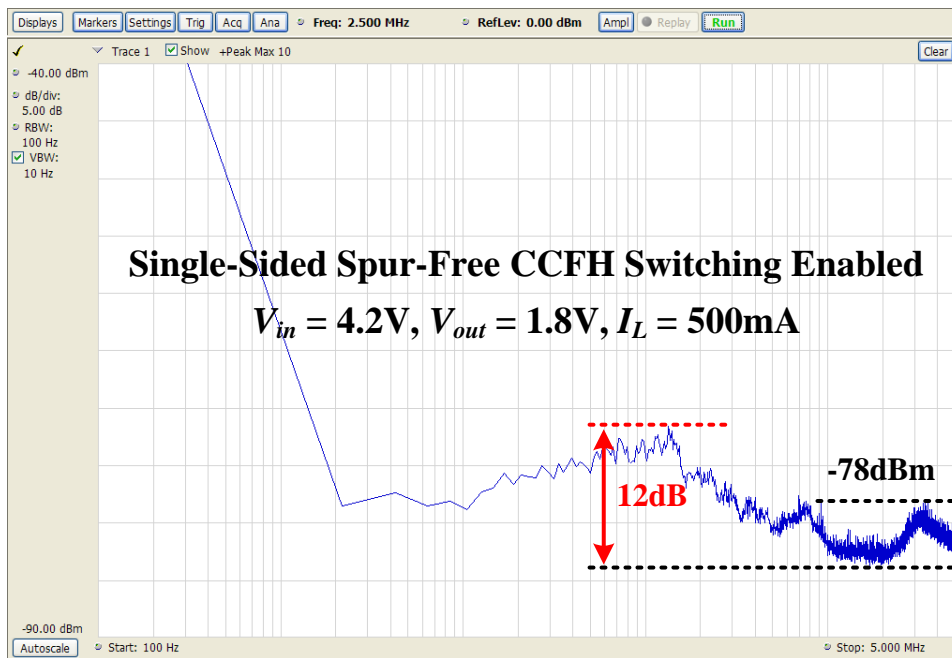


(b)

Figure 6.16 Spur-free CCFH switching disabled (i.e. single switching frequency): (a) Output voltage ripple, and (b) Low-frequency spectrum up to 5 MHz.

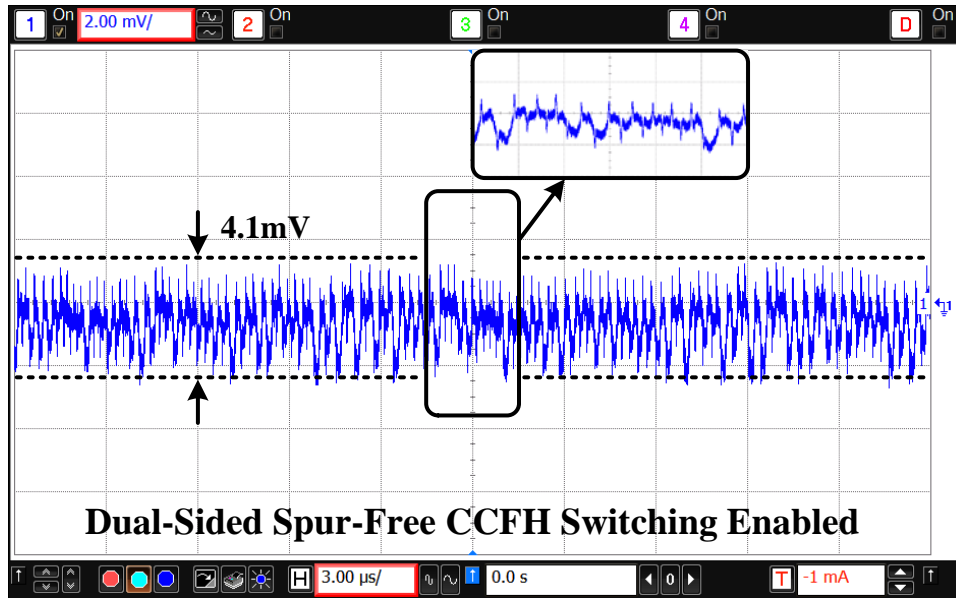


(a)

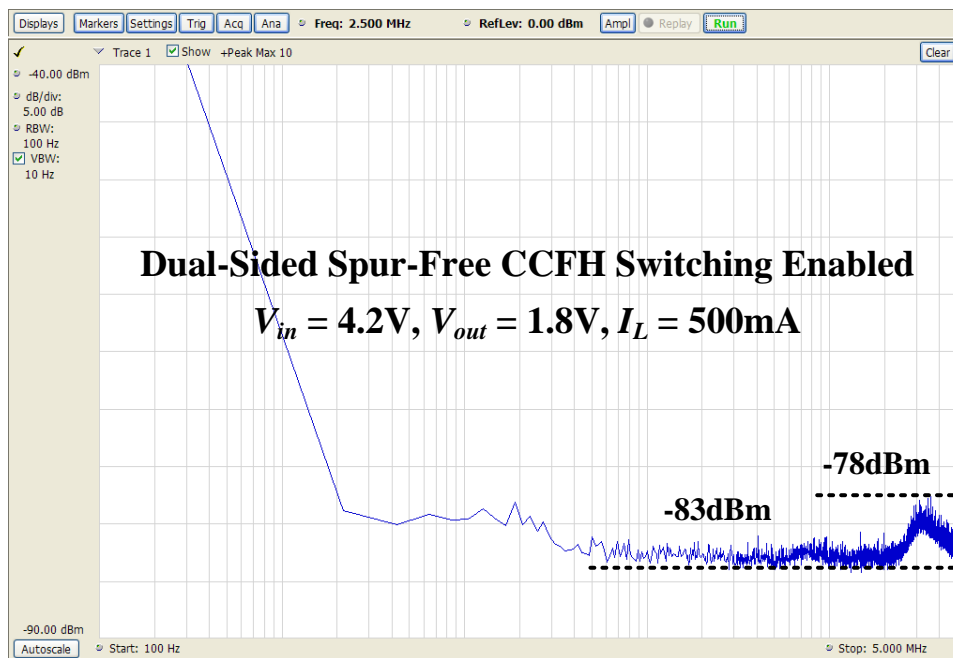


(b)

Figure 6.17 Spur-free CCFH switching with single-sided band modulation: (a) Output voltage ripple, and (b) Low-frequency spectrum up to 5 MHz.



(a)



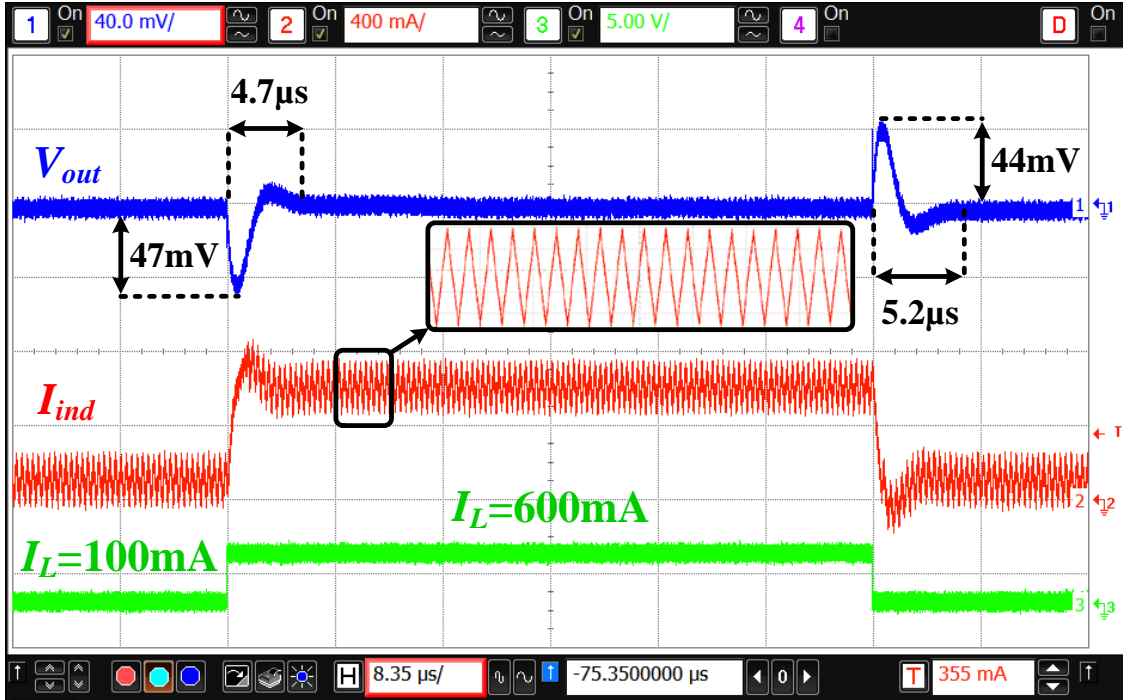
(b)

Figure 6.18 Spur-free CCFH switching with dual-sided band modulation: (a) Output voltage ripple, and (b) Low-frequency spectrum up to 5 MHz.

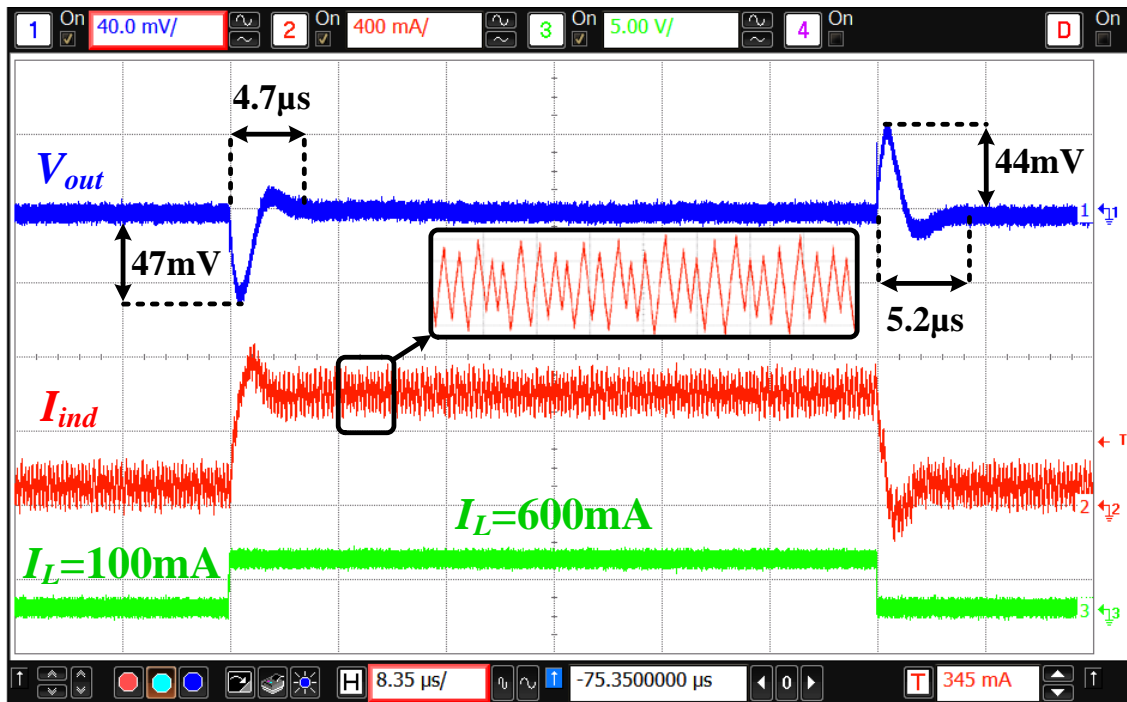
The transient response of the converter is also measured using a 500-mA load step with and without the proposed spur-free CCFH. As shown in Fig. 6.19, the response of the converter is almost identical in both cases, which indicates that incorporating spur-free CCFH has minimal impact on the transient response, whether in steady-state as in Fig. 6.18, or in load transient conditions as in Fig. 6.19.

To demonstrate the effectiveness of the proposed feedforward adaptive hysteretic band control in reducing switching frequency variability with the input voltage, the switching frequency of the converter is measured versus the input voltage with and without the feedforward controller. The switching frequency versus the input voltage is shown for both cases in Fig. 6.20, where the normalized deviation $2(f_{s(max)} - f_{s(min)}) / (f_{s(max)} + f_{s(min)})$ is reduced from 64% to 21% at 1.8-V output, and from 26% to 14% at 1.2-V output.

To demonstrate the operation of the proposed all-digital soft-startup circuit, a conventional analog soft-startup circuit with an off-chip capacitor is also implemented in the same chip for performance comparison purposes. The operation of the soft-startup circuit is tested by periodically enabling and disabling the converter and measuring the output voltage and inductor current as shown in Fig. 6.21. As seen, both circuits yield similar performance. However, the proposed circuit is faster and has the advantage of being purely digital with no large on-chip or off-chip capacitances. Therefore, it can be easily tweaked to meet the required performance without extensive design modifications. The converter's power conversion efficiency is measured versus load current at various output voltages with and without spur-free CCFH as shown in Fig. 6.22 with an input voltage of 3.6V and Fig. 6.23 with an input voltage of 4.2V, where the peak efficiency is 92% and the degradation in efficiency due to spur-free CCFH switching is less than 0.7%.



(a)



(b)

Figure 6.19 Output transient response to a 500-mA load step with: (a) Spur-free CCFH switching disabled (i.e. single switching frequency), and (b) Spur-free CCFH switching enabled. Input voltage 4.2 V, output voltage 1.8 V.

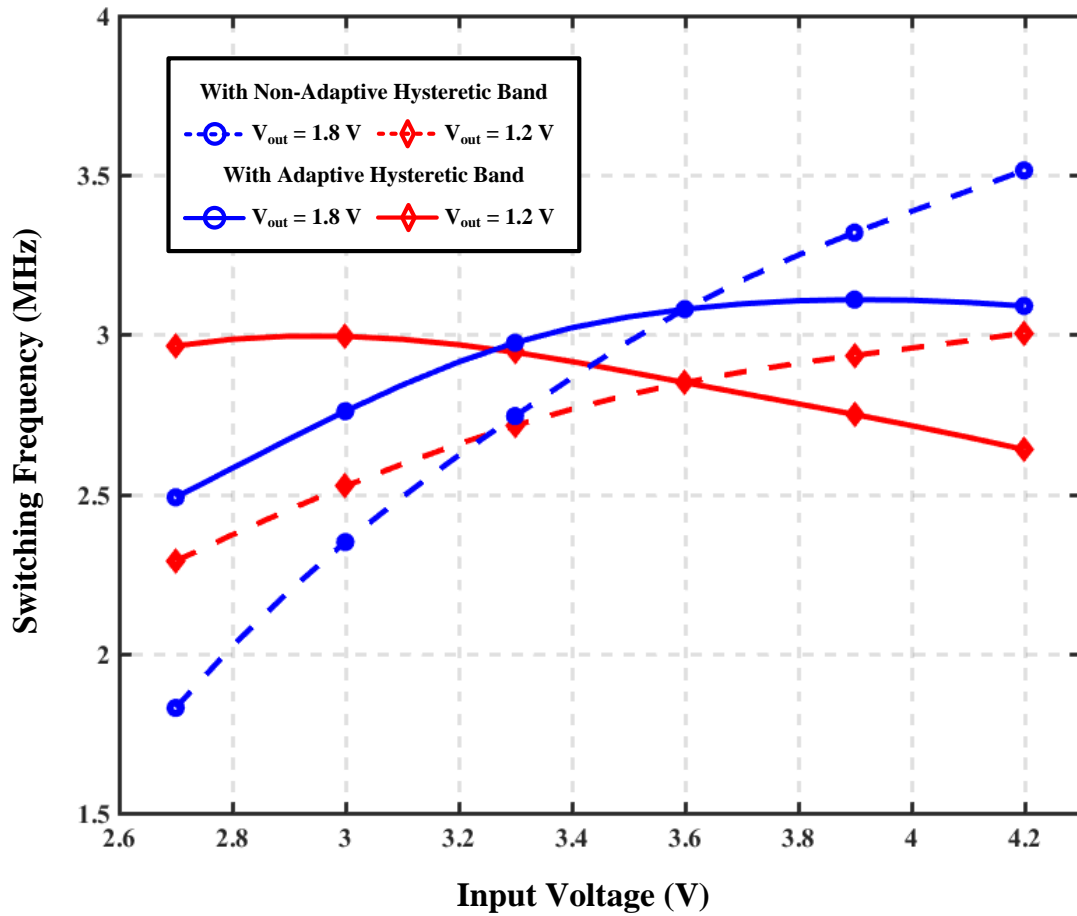
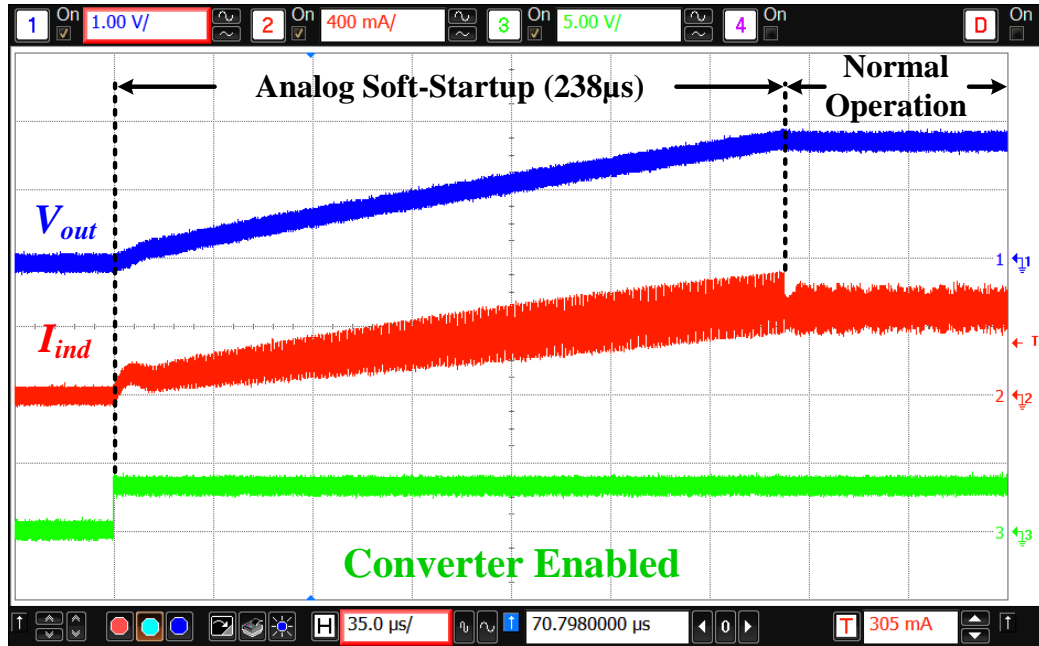
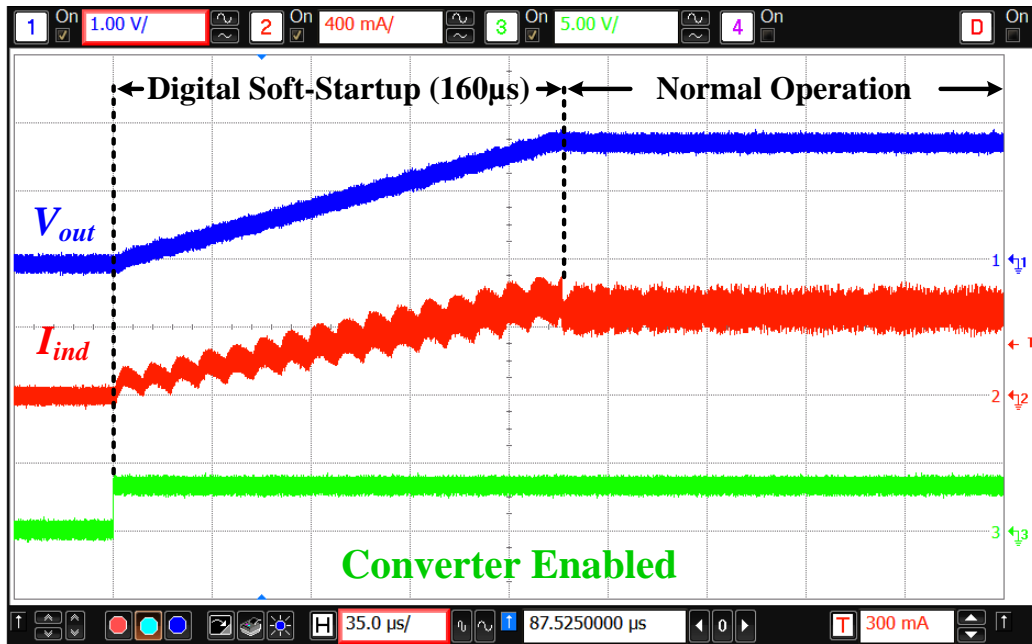


Figure 6.20 Switching frequency versus input voltage at different output voltages with and without adaptive hysteresis band.



(a)



(b)

Figure 6.21 Startup operation of the converter with: (a) A conventional analog soft-startup circuit, and (b) The proposed all-digital soft-startup. Input voltage 4.2 V, output voltage 1.8 V, load current 500 mA.

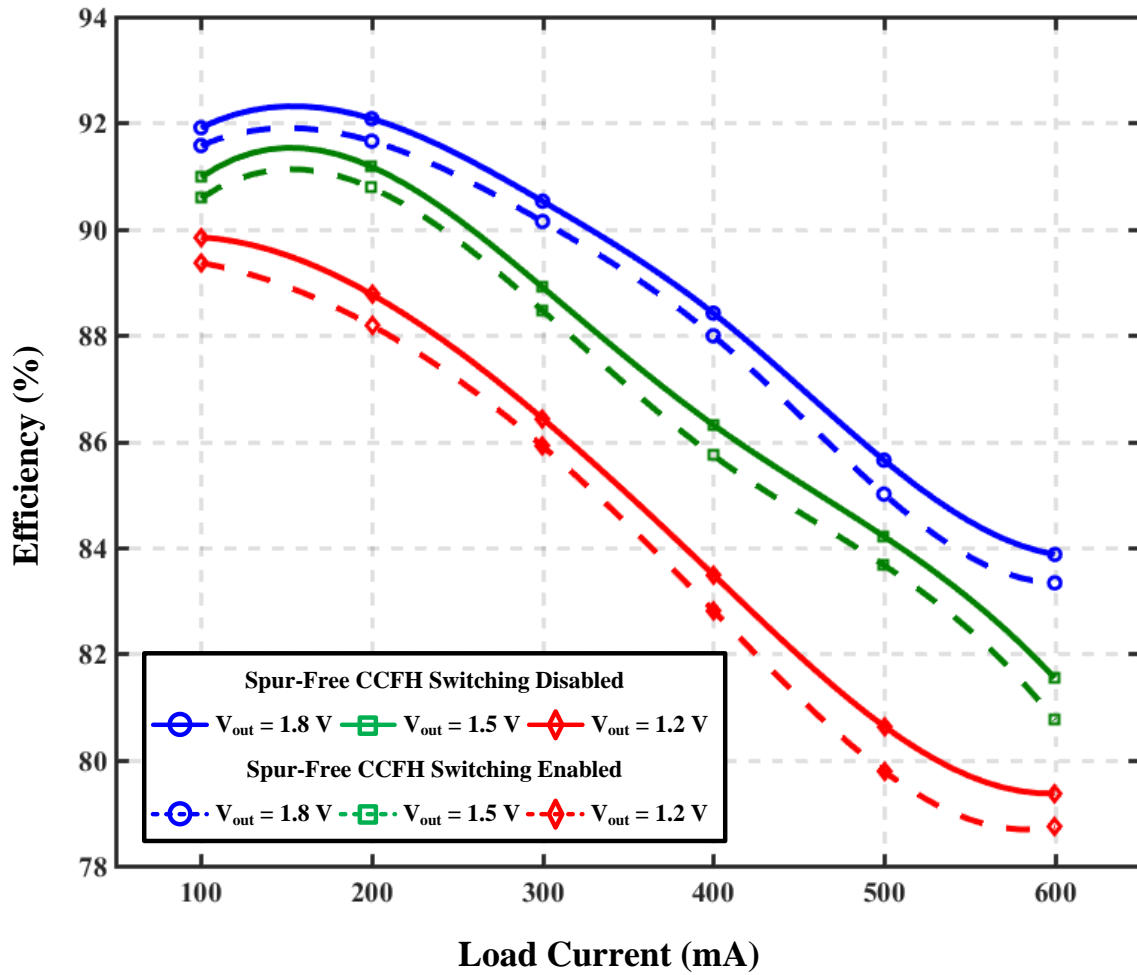


Figure 6.22 Power conversion efficiency versus load current at different output voltages with and without the proposed spur-free CCFH switching. Input voltage 3.6 V.

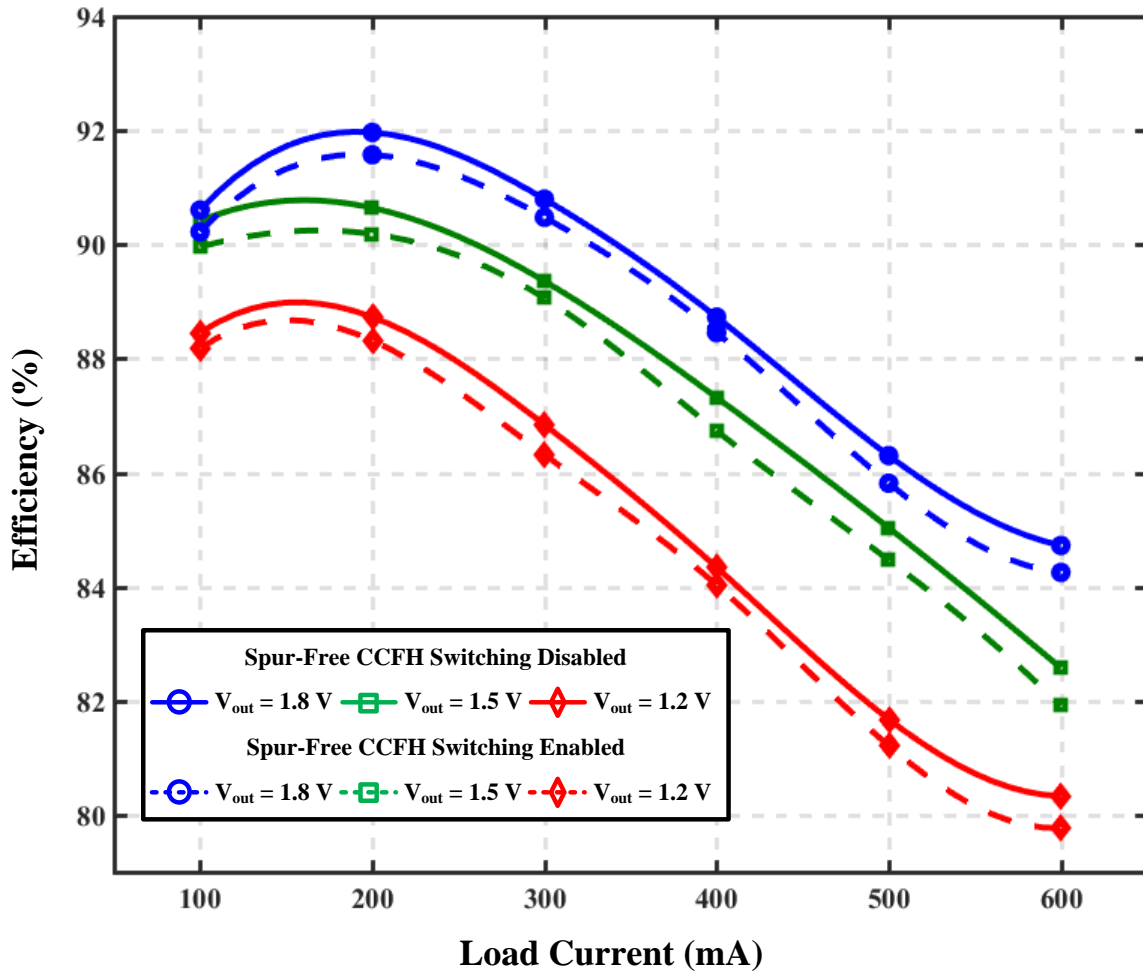


Figure 6.23 Power conversion efficiency versus load current at different output voltages with and without the proposed spur-free CCFH switching. Input voltage 4.2 V.

Table 6.1 Performance summary and comparison.

	This Work	TPEL 2013 [11]	TVLSI 2013 [36]	TVLSI 2012 [12]	SOVC 2012 [13]	SOVC 2011 [14]	ISSCC 2009 [15]	
Control Scheme	Current-Mode Hysteretic with Feedforward Adaptive Band Control and Spur-Free CCFH	Current-Mode Hysteretic	Voltage-Mode PWM with Spur-Free CCFH	Pseudo-PWM Voltage-Mode Hysteretic	Hybrid Voltage/Current-Mode Hysteretic	ΔI_L -Emulated Hysteretic	Quasi- V^2 (Current-Mode) Hysteretic	
Technology	0.35- μ m CMOS	130-nm CMOS	0.35- μ m CMOS	0.35- μ m CMOS	130-nm CMOS	0.35- μ m CMOS	0.35- μ m CMOS	
Active Silicon Area	0.9 mm ²	0.732 mm ²	0.36 mm ² *	4.18 mm ² **	0.7 mm ²	1.3 mm ²	1.8 mm ² **	
Input Voltage	2.7–4.2 V	2.4–4.8 V	3.3–5.5 V	2.4–4.2 V	2.5 V	3 V	2.7–3.3 V	
Output Voltage	1.2–1.8 V	1.8 V	1.3–3.8 V	1.8 V	0.7–1.8 V	0.9–2.1 V	0.9–2.1 V	
Maximum Load	600 mA	2 A	600 mA	500 mA	900 mA	800 mA	500 mA	
Inductor	2.2 μ H	330 nH	2.2 μ H	4.7 μ H	1–5 μ H	4.7 μ H	2.2 μ H	
Output Capacitor	4.7 μ F	10 μ F	10 μ F	4.7 μ F	10 μ F	9.1 μ F	4.4 μ F	
Frequency Regulation Scheme	Eliminated	Analog PLL	None (PWM control)	Analog PLL	Digital Frequency Regulation Loop	Digital Adaptive Frequency Control	Digital Frequency Locked Loop (FLL)	
Switching Frequency	Hopped: 2.5 MHz $\leq f_{s(avg)} \leq$ 3.1 MHz	Regulated at 3.2 MHz	Hopped: $f_{s(avg)} =$ 4.75 MHz	Regulated at 1 MHz	Regulated at 1 MHz	Regulated at 1.7 MHz	Regulated at 3 MHz	
Spur-Free Spectrum	Yes	No	Yes	No	No	No	No	
Peak Efficiency	92%	89%	90%	95%	93%	92.7%	93%	
Load Step Response	Load Step (All)	500 mA (@ $V_{in} = 4.2$ V, $V_{out} = 1.8$ V)	1 A (@ $V_{in} = 3.6$ V)	200 mA (@ $V_{in} = 4.2$ V, $V_{out} = 1.8$ V)	200 mA (@ $V_{in} = 3.3$ V)	600 mA (@ $V_{out} = 1.2$ V, $L = 1.8$ μ H)	400 mA (@ $V_{out} = 0.9$ V)	450 mA (@ $V_{in} = 3$ V)
	Undershoot/Overshoot	47 mV / 44 mV	40 mV / 60 mV	70 mV / 120 mV	40 mV / 40 mV	61 mV / 72 mV	35 mV / 52 mV	38 mV / 45 mV (@ $V_{out} = 0.9$ V) 72 mV / 40 mV (@ $V_{out} = 2.1$ V)
	Recovery Time	4.7 μ s / 5.2 μ s	12 μ s / 12 μ s	58 μ s / 54 μ s	5 μ s / 5 μ s	< 10 μ s	7.6 μ s / 14.4 μ s	2.4 μ s / 2.8 μ s (@ $V_{out} = 0.9$ V) 10 μ s / 7.2 μ s (@ $V_{out} = 2.1$ V)

* Requires off-chip compensation.

** Total chip area with pads.

Table 6.1 summarizes the key performance and design aspects of the proposed converter versus existing literature. Compared to spur-free CCFH converters with PWM control [36], the proposed spur-free CCFH hysteretic converter offers much better transient load regulation with significantly smaller overshoot/undershoot and faster recovery time without compromising spur-free operation. Compared to other hysteretic controllers [11-15], it offers superior noise performance by eliminating spurs at every node within the converter without compromising the efficiency or dynamic performance expected from hysteretic controllers.

CHAPTER 7

FUTURE WORK AND CONCLUSION

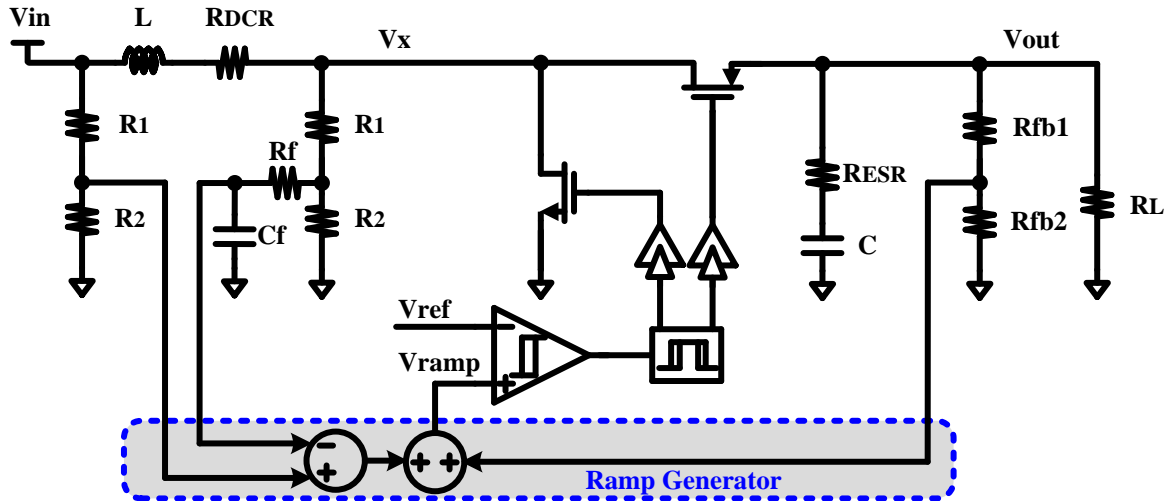
The future work for extending the spur-free current-mode hysteretic control to boost converters along with the preliminary simulation results are presented in this chapter as well as the final conclusion.

7.1 Spur-Free Current-Mode Hysteretic Boost Converter

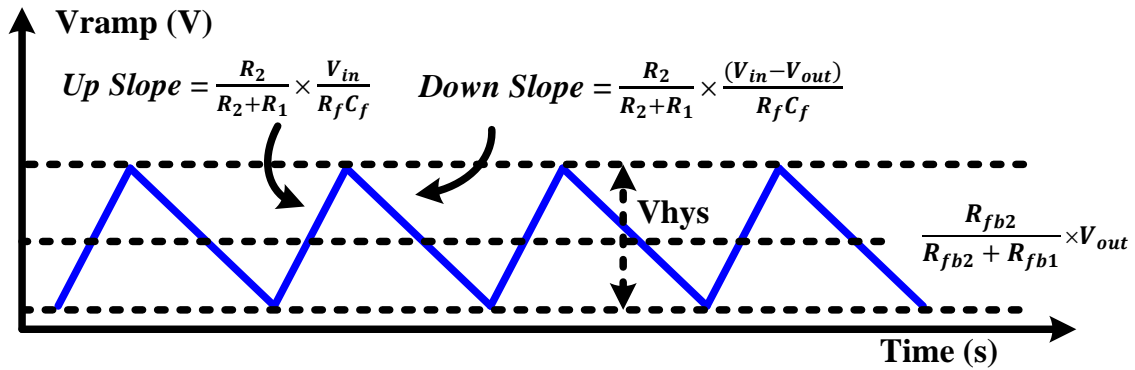
Boost converters are step-up inductor-based switching power regulators that are employed in different applications like energy-harvesting systems, light-emitting diodes (LED) drivers, and power supply tracking for RF power amplifiers [48, 49]. The block diagram of an emulated-ramp feedback (ERF) current-mode hysteretic boost converter is shown in Fig. 7.1 along with the associated waveforms [50]. The control scheme consists of a single control loop where the average of the ramp signal (V_{ramp}) corresponds to the average output voltage while its AC component corresponds to the inductor current ripple as shown in Fig. 7.1(b) which makes it a suitable architecture for implementing spur-free switching control. As a self-oscillating architecture, the switching frequency of the converter varies with the operating conditions. In fact, the switching frequency can be expressed as:

$$f_s = \left(\frac{R_2}{R_1 + R_2} \right) \times \frac{V_{in} \left(1 - \frac{V_{in}}{V_{out}} \right)}{(R_f C_f) \times V_{hys}} \quad (7.1)$$

where V_{in} , V_{out} are the input and output voltages, V_{hys} is the hysteretic band of the comparator, $R_f C_f$ is the time constant of the RC filter and R_1 , R_2 are the resistors forming the voltage divider at the input voltage and switching node (V_x).



(a)



(b)

Figure 7.1 (a) Current-mode hysteretic boost converter architecture proposed in [50], (b) Emulated ramp signal waveform.

An attempt to employ spur-free switching to the ERF current-mode hysteretic boost converter is shown in Fig. 7.2 where the hysteretic band of the hysteretic comparator is randomly hopped among a set of M value, such that the ratios of the different hysteretic bands meet the spur-elimination condition. Preliminary simulation results demonstrate the elimination of spurious tones by hopping among 8 different hysteretic bands at different operating conditions as shown in Fig. 7.3.

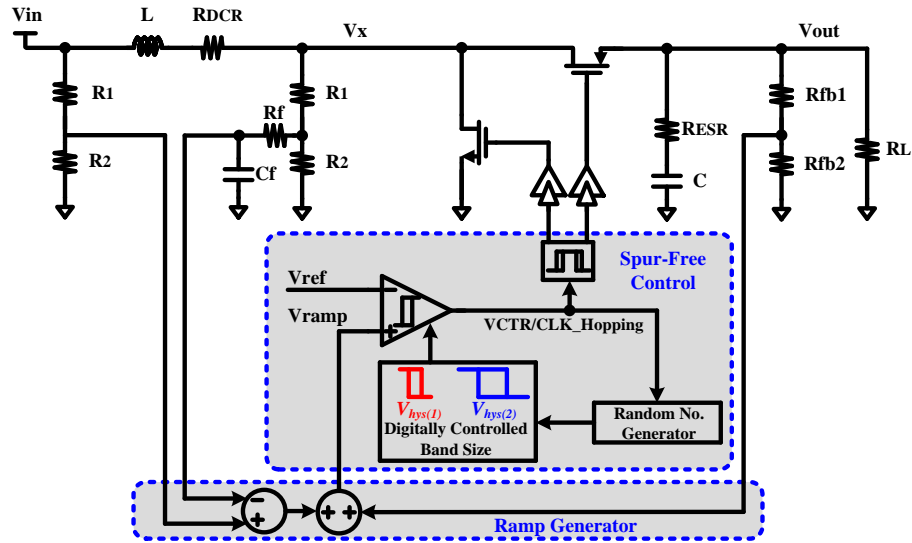


Figure 7.2 Proposed spur-free current-mode hysteretic boost converter.

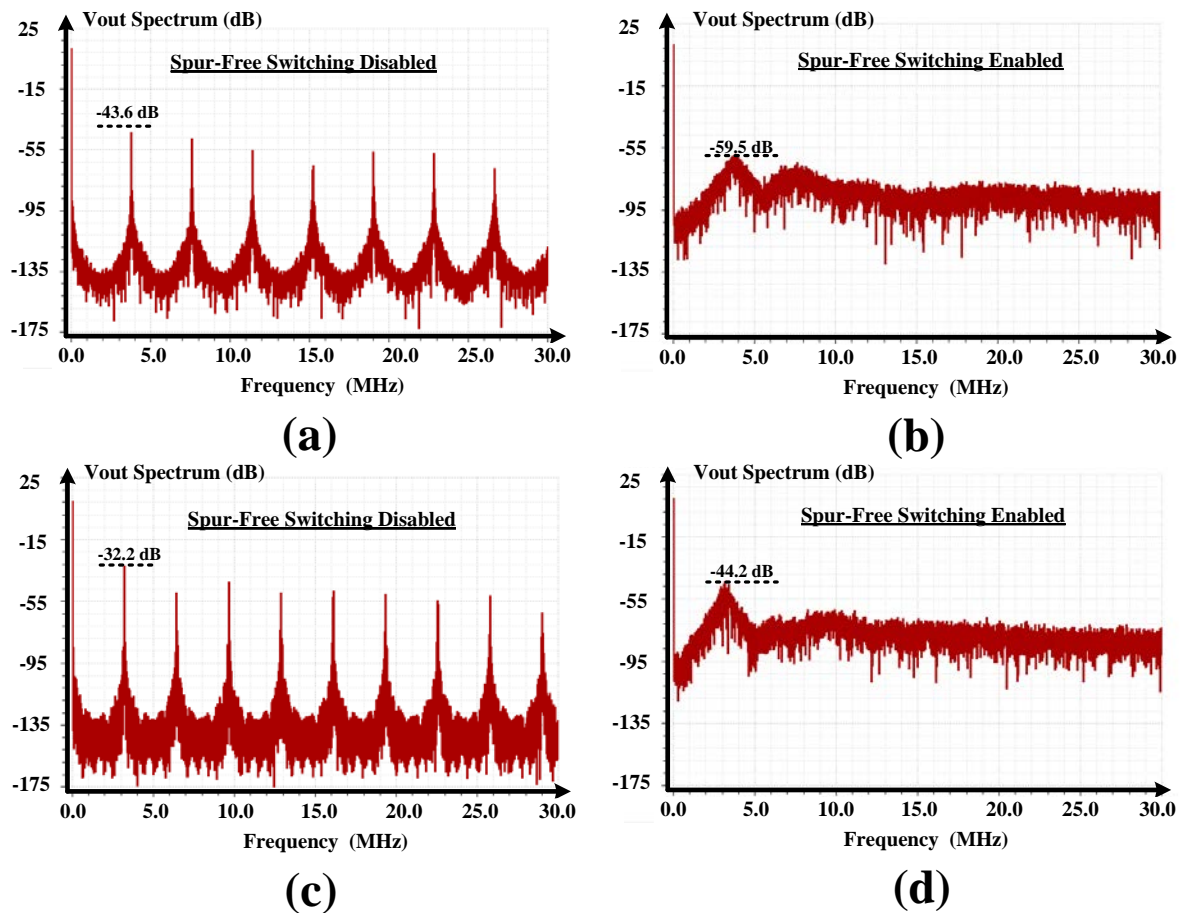


Figure 7.3 Output spectrum with: (a) A single hysteric band, (b) Spur-free switching with 8 hysteric bands operating at 2.7V input, 3.6V output, 300mA load. (c) A single hysteric band and, (d) Spur-free switching with 8 hysteric bands operating at 1.8V input, 3V output, 200mA load.

7.2 Conclusion

A spur-free current-mode hysteretic buck converter with spur-free CCFH switching was presented. The converter fully eliminates spurious noise irrespective of variability in operating conditions and switching frequency. Thus, it enables hysteretic topologies to be used to power noise-sensitive loads, or to be integrated within noise-sensitive systems without requiring frequency regulation loops or compromising the superior dynamic response of hysteretic converters. The proposed realization of the spur-free CCFH switching scheme using dual-sided band modulation eliminates inductor current imbalance due to hopping, and thus eliminates the output glitches and the low-frequency noise floor peaking typically associated with frequency hopping. Furthermore, the feedforward adaptive hysteretic band control reduces the variations in the converter's average switching frequency with the input voltage, while the all-digital soft-startup circuit limits in-rush current without requiring off-chip components. The converter was fabricated in a 0.35- μm standard CMOS technology, and it achieves 92% peak efficiency.

REFERENCE:

- [1] Wei Fu and Ayman Fayed, "Power Conversion Schemes in Mixed-Signal SoCs," *IEEE Int. symposium on circuits and Systems (ISCAS 2014)*, pp. 606-609, Melbourne, Australia, June 2014.
- [2] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.
- [3] R. Redl and J. Sun, "Ripple-Based Control of Switching Regulators—An Overview," in *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2669-2680, Dec. 2009.
- [4] J. H. Chen, P. J. Liu, Y. L. Hung, H. S. Yang and Y. J. E. Chen, "A Spur-Reduced Multimode Power-Level Tracking Power Amplifier Using a Frequency-Hopping DC–DC Converter," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1333-1338, May 2010.
- [5] Jau-Horng Chen, Pang-Jung Liu and Y. J. E. Chen, "A spurious emission reduction technique for power amplifiers using frequency hopping DC-DC converters," *2009 IEEE Radio Frequency Integrated Circuits Symposium*, Boston, MA, 2009, pp. 145-148.
- [6] C. Tao and A. A. Fayed, "A GSM Power Amplifier Directly-Powered From a DC-DC Power Converter," in *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 1, pp. 38-40, Jan. 2012.
- [7] T. Szepesi, "Stabilizing the Frequency of Hysteretic Current-Mode DC/DC Converters," in *IEEE Transactions on Power Electronics*, vol. PE-2, no. 4, pp. 302-312, Oct. 1987.

- [8] F. Su, W. H. Ki and C. Y. Tsui, "Ultra Fast Fixed-Frequency Hysteretic Buck Converter With Maximum Charging Current Control and Adaptive Delay Compensation for DVS Applications," in *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 815-822, April 2008.
- [9] P. Li, D. Bhatia, L. Xue and R. Bashirullah, "A 90–240 MHz Hysteretic Controlled DC-DC Buck Converter With Digital Phase Locked Loop Synchronization," in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2108-2119, Sept. 2011.
- [10] M. K. Song, M. F. Dehghanpour, J. Sankman and D. Ma, "A VHF-level fully integrated multi-phase switching converter using bond-wire inductors, on-chip decoupling capacitors and DLL phase synchronization," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014, pp. 1422-1425.
- [11] B. Labbe, B. Allard, X. Lin-Shi and D. Chesneau, "An Integrated Sliding-Mode Buck Converter With Switching Frequency Control for Battery-Powered Applications," in *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4318-4326, Sept. 2013.
- [12] Y. Zheng, H. Chen and K. N. Leung, "A Fast-Response Pseudo-PWM Buck Converter With PLL-Based Hysteresis Control," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 7, pp. 1167-1174, July 2012.
- [13] Q. Khan, A. Elshazly, S. Rao, R. Inti and P. K. Hanumolu, "A 900mA 93% efficient 50 μ A quiescent current fixed frequency hysteretic buck converter using a highly digital hybrid voltage- and current-mode control," *2012 Symposium on VLSI Circuits (VLSIC)*, Honolulu, HI, 2012, pp. 182-183.

- [14] H. Chen and D. Ma, "A fast-transient DVS-capable switching converter with ΔI_L -emulated hysteretic control," *VLSI Circuits (VLSIC), 2011 Symposium on*, Honolulu, HI, 2011, pp. 282-283.
- [15] F. Su and W. H. Ki, "Digitally assisted quasi-V2 hysteretic buck converter with fixed frequency and without using large-ESR capacitor," *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, San Francisco, CA, 2009, pp. 446-447,447a.
- [16] *TPS62660 Datasheet*, Texas Instruments, Dallas, TX, 2010. Available online at: <http://www.ti.com/lit/ds/symlink/tps62660.pdf>
- [17] *LTC3770 Datasheet*, Linear Technology, Milpitas, CA, 2011. Available online at: <http://www.linear.com/docs/en/datasheet/3770fc.pdf>
- [18] Y. Wen and O. Trescases, "Analysis and Comparison of Frequency Stabilization Loops in Self-Oscillating Current Mode DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4753-4766, Oct. 2013.
- [19] J. S. Chang, H. S. Oh, Y. H. Jun and B. S. Kong, "Fast Output Voltage-Regulated PWM Buck Converter With an Adaptive Ramp Amplitude Control," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 10, pp. 712-716, Oct. 2013.
- [20] M. Nashed and A. Fayed, "Variable switching noise mitigation in hysteretic power converters using spur-free control," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 410-413.

- [21] G. A. Rincon-Mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," in *IEEE Journal of Solid-State Circuits*, vol. 33, no. 1, pp. 36-44, Jan 1998.
- [22] J. N. Kitchen, C. Chu, S. Kiaei and B. Bakkaloglu, "Combined Linear and Δ -Modulated Switch-Mode PA Supply Modulator for Polar Transmitters," in *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 404-413, Feb. 2009.
- [23] Y. K. Ramadass, A. A. Fayed and A. P. Chandrakasan, "A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45 nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2557-2565, Dec. 2010.
- [24] F. Su and W. H. Ki, "Component-Efficient Multiphase Switched-Capacitor DC-DC Converter With Configurable Conversion Ratios for LCD Driver Applications," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 8, pp. 753-757, Aug. 2008.
- [25] Ngok-Man Sze, Feng Su, Yat-Hei Lam, Wing-Hung Ki and Chi-Ying Tsui, "Integrated single-inductor dual-input dual-output boost converter for energy harvesting applications," *2008 IEEE International Symposium on Circuits and Systems*, Seattle, WA, 2008, pp. 2218-2221.
- [26] J. A. Starzyk, Ying-Wei Jan and Fengjing Qiu, "A DC-DC charge pump design based on voltage doublers," in *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 3, pp. 350-359, Mar 2001.

- [27] C. Tao and A. Fayed, "Analysis and modelling of buck converters output spectrum in CCM with PWM control," *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Seoul, 2011, pp. 1-4.
- [28] V. Gupta, G. A. Rincon-Mora and P. Raha, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," *SOC Conference, 2004. Proceedings. IEEE International*, 2004, pp. 311-315.
- [29] N. K. Poon, J. C. P. Liu, C. K. Tse and M. H. Pong, "Techniques for input ripple current cancellation: classification and implementation [in SMPS]," in *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1144-1152, Nov 2000.
- [30] S. Abedinpour, B. Bakkaloglu and S. Kiaei, "A Multistage Interleaved Synchronous Buck Converter With Integrated Output Filter in 0.18 μm SiGe Process," in *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2164-2175, Nov. 2007.
- [31] S. K. Dunlap and T. S. Fiez, "A noise-shaped switching power supply using a delta-sigma modulator," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 6, pp. 1051-1061, June 2004.
- [32] M. K. Alghamdi and A. A. Hamoui, "A Spurious-Free Switching Buck Converter Achieving Enhanced Light-Load Efficiency by Using a Δ -Modulator Controller With a Scalable Sampling Frequency," in *IEEE Journal of Solid-State Circuits*, vol. 47, no. 4, pp. 841-851, April 2012.
- [33] E. J. Kim, C. H. Cho, W. Kim, C. H. Lee and J. Laskar, "Spurious noise reduction by modulating switching frequency in DC-to-DC converter for RF power amplifier," *2010 IEEE Radio Frequency Integrated Circuits Symposium*, Anaheim, CA, 2010, pp. 43-46.

- [34] C. Tao and A. A. Fayed, "A Buck Converter With Reduced Output Spurs Using Asynchronous Frequency Hopping," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 11, pp. 709-713, Nov. 2011.
- [35] K. K. Tse, H. S. H. Chung, S. Y. Huo and H. C. So, "Analysis and spectral characteristics of a spread-spectrum technique for conducted EMI suppression," in *IEEE Transactions on Power Electronics*, vol. 15, no. 2, pp. 399-410, Mar 2000.
- [36] C. Tao and A. A. Fayed, "PWM Control Architecture With Constant Cycle Frequency Hopping and Phase Chopping for Spur-Free Operation in Buck Regulators," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 9, pp. 1596-1607, Sept. 2013.
- [37] C. Tao and A. A. Fayed, "Spurious-noise-free buck regulator for direct powering of analog/RF loads using PWM control with random frequency hopping and random phase chopping," *2011 IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2011, pp. 396-398.
- [38] C. Tao and A. A. Fayed, "A Low-Noise PFM-Controlled Buck Converter for Low-Power Applications," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 12, pp. 3071-3080, Dec. 2012.
- [39] Chin Chang, "Lossless current sensing and its application in current mode control," *2008 IEEE Power Electronics Specialists Conference*, Rhodes, 2008, pp. 4086-4091.
- [40] P. J. Liu, J. N. Tai, H. S. Chen, J. H. Chen and Y. J. E. Chen, "Spur-Reduction Design of Frequency-Hopping DC-DC Converters," in *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4763-4771, Nov. 2012.

- [41] E. N. Y. Ho and P. K. T. Mok, "Design of PWM Ramp Signal in Voltage-Mode CCM Random Switching Frequency Buck Converter for Conductive EMI Reduction," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 2, pp. 505-515, Feb. 2013.
- [42] B. Labbe, D. Chesneau, B. Allard and X. Lin-Shi, "Modeling and design of an integrated sliding-mode buck converter with regulated switching frequency suitable for mobile devices," *ECCE Asia Downunder (ECCE Asia), 2013 IEEE*, Melbourne, VIC, 2013, pp. 893-899.
- [43] Y. Wang and D. Ma, "A 450-mV Single-Fuel-Cell Power Management Unit With Switch-Mode Quasi- V^2 Hysteretic Control and Automatic Startup on 0.35- μm Standard CMOS Process," in *IEEE Journal of Solid-State Circuits*, vol. 47, no. 9, pp. 2216-2226, Sept. 2012.
- [44] W. R. Liou, M. L. Yeh and Y. L. Kuo, "A High Efficiency Dual-Mode Buck Converter IC For Portable Applications," in *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 667-677, March 2008.
- [45] W. Yan, W. Li and R. Liu, "A Noise-Shaped Buck DC-DC Converter With Improved Light-Load Efficiency and Fast Transient Response," in *IEEE Transactions on Power Electronics*, vol. 26, no. 12, pp. 3908-3924, Dec. 2011.
- [46] D. Johns and K. Martin, *Analog Integrated Circuit Design*. John Wiley, 1997.
- [47] Changsik Yoo, "A CMOS buffer without short-circuit power consumption," in *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 9, pp. 935-937, Sep 2000.

- [48] D. Kang, D. Kim, J. Choi, J. Kim, Y. Cho and B. Kim, "A Multimode/Multiband Power Amplifier With a Boosted Supply Modulator," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 10, pp. 2598-2608, Oct. 2010.
- [49] X. Jing and P. K. T. Mok, "A Fast Fixed-Frequency Adaptive-On-Time Boost Converter With Light Load Efficiency Enhancement and Predictable Noise Spectrum," in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2442-2456, Oct. 2013.
- [50] J. S. Guo, S. M. Lin and C. H. Tsai, "A hysteretic boost regulator with Emulated-Ramp Feedback (ERF) current-sensing technique for LED driving applications," *Solid-State Circuits Conference (A-SSCC), 2013 IEEE Asian*, Singapore, 2013, pp. 61-64.